32Gb B-die NAND Flash

Multi-Level-Cell (2bit/cell)

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Revision History

Revision No.	History	Draft Date	Remark	Edited by	Reviewed by
0.0	1. Initial issue	Jul. 14, 2011	Target	Y.E.Yoon	Y.E.Yoon
0.1	1. Chpater 1.1 Features updated. 2. Chpater 1.2 Product List updated. 3. Chpater 1.3 General Description revised. 4. Chpater 1.4 Pin Configuration (48TSOP) updated. 5. Chpater 2.1 Absolute Maximum DC Rating added. 6. Chpater 2.2 Recommended Operating Conditions revised. 7. Chpater 2.3 DC And Operating Characteristics revised. 8. Chpater 2.4 Valid Block revised. 9. Chpater 2.5 AC Test Condition revised. 10. Chpater 2.6 Capacitance revised. 11 Chpater 2.8 Program / Erase Characteristics revised. 12.Chpater 2.10 AC Characteristics for Operation revised. 13.Chpater 4.26 00h Address ID Cycle revised. 14.Chpater 4.27 40h Address ID Cycle revised. 15.Chpater 5.18 Read Id revised.	Oct. 31, 2011	Target	H.H.Shin	H.K.Kim
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1.0	1. There is no change.	Mar. 07, 2012	Target	H.H.Shin	H.K.Kim

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1.0 INTRODUCTION

1.1 Features

- Voltage Supply :
  - VCC : 3.3V (2.7V ~ 3.6V)
  - VccQ : 3.3V (2.7V ~ 3.6V)
- Organization of Single die
  - Page Size : (8K + 1K) x 8bit
  - Data Register : (8K + 1K) x 8bit
  - Block Size : (1M + 128K) bytes
  - Unit Device Capacity: (4096M + 512M)bytes
- Products
  - K9GBG08U0B: Unit device x 1
  - K9LCG08U0B: Unit device x 2
- Automatic Program and Erase
  - Page Program : (8K + 1K)Byte
  - Block Erase : (1M + 128K)Byte
- Page Read Operation
  - Random Read(tR) : 80us(Max)
  - Serial Access : 25ns(Min.)
- Write Cycle Time
  - Page Program time : 1.3ms(Typ.)
  - Block Erase Time : 5ms(Typ.)
- Command/Address/Data Multiplexed I/OPort
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
- ECC Requirement : 40bits/ (1K+128)byte
- Randomizer function required by Controller

- Unique ID for Copyright Protection.
- Package
- K9GBG08U0B-SCB0 : Pb/Halogen Free Package
  48-Pin TSOP (12 x 20 / 1.00 mm pitch)
- K9LCG08U0B-SCB0 : Pb/Halogen Free Package
  48-Pin TSOP (12 x 20 / 1.00 mm pitch)

1.2 Product List

Part Number	Density	Interface	Organization	Vcc Range	VccQ Range	PKG Type
K9GBG08U0B	32Gb	Conventional	x8	2.7V ~ 3.6V	2.7V ~ 3.6V	48TSOP
K9LCG08U0B	64Gb					

1.3 General Description

The device is offered in 3.3V Vcc. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. A program operation can be performed in typical 1.3ms on the 8,704-byte page and an erase operation can be performed in typical 5ms on a (1M+128K)byte block. Data in the data register can be read out at 25ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the K9XXG08U0B's extended reliability of P/E cycles which are presented in the Qualification report by providing ECC(Error Correcting Code) with real time mapping-out algorithm. The K9XXG08U0B is an optimum solution for large nonvolatile storage applications such as solid state file storage and other portable applications requiring non-volatility.

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1.4 Pin Configuration (48TSOP)

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Left Pin	#		#	Right Pin
Vcc	1		48	Vss
Vss	2		47	N.C
N.C	3		46	N.C
N.C	4		45	N.C
N.C	5		44	I/O7
N.C	6		43	I/O6
R/B	7		42	I/O5
RE	8		41	I/O4
CE	9		40	N.C
N.C	10		39	N.C
N.C	11		38	VccQ
Vcc	12		37	Vcc
Vss	13		36	Vss
N.C	14		35	N.C
N.C	15		34	VccQ
CLE	16		33	N.C
ALE	17		32	I/O3
WE	18		31	I/O2
WP	19		30	I/O1
N.C	20		29	I/O0
N.C	21		28	N.C
N.C	22		27	N.C
Vss	23		26	N.C
Vcc	24		25	Vss

48-pin TSOP1
Standard Type
12mm x 20mm

1.4.1 Package Dimensions

48-PIN LEAD FREE PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)

48 - TSOP1 - 1220AF   Unit :mm/Inch

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1.5 Pin Description

Pin Name	Pin Function
I/O$_0$ ~ I/O$_7$	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the $\overline{WE}$ signal.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of $\overline{WE}$ with ALE high.
$\overline{CE}$	**CHIP ENABLE** The $\overline{CE}$ input is the device selection control. When the device is in the Busy state, $\overline{CE}$ high is ignored, and the device does not return to standby mode in program or erase operation.
$\overline{RE}$	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.
$\overline{WE}$	**WRITE ENABLE** The $\overline{WE}$ input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the $\overline{WE}$ pulse.
$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin provides inadvertent program/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{WP}$ pin is active low.
R/$\overline{B}$	**READY/BUSY OUTPUT** The R/$\overline{B}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
Vcc	**POWER** V$_{CC}$ is the power supply for device.
VccQ	**I/O POWER** The VccQ is the power supply for input and/or output signals.
Vss	**GROUND**
VssQ	**I/O GROUND** The VssQ is the power supply ground
N.C	**NO CONNECTION** Lead is not internally connected.

NOTE :
Connect all VCC and VSS pins of each device to common power supply outputs.
Do not leave VCC or VSS disconnected.

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Functional Block Diagram
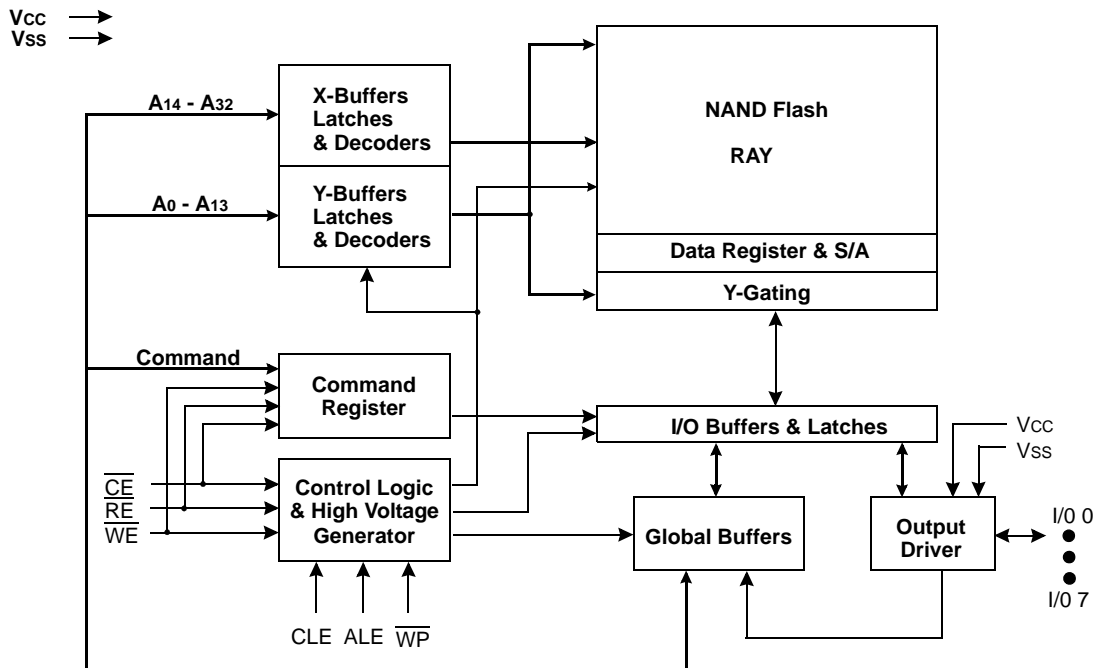
Array Organization of Unit Device

1 Page = (8K + 1K)Bytes
1 Block = 128 Pages
= (8K+1K) Bytes x 128Pages
= (1M + 128K) Bytes

512K Pages
(=4,096 Blocks)

Unit Device = 4,096 Blocks
= 4,096 x (1M+128K) Bytes
= 36,864 Mbits

8 bit

Page Register   Page Register   I/O 0 ~ I/O 7

8K Bytes   1K Bytes
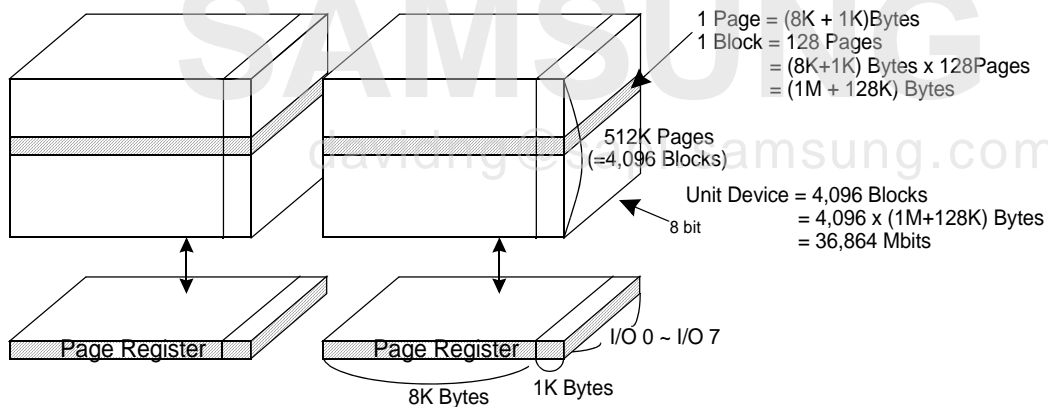
	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st Cycle	$A_0^{(1)}$	A_1	A_2	A_3	A_4	A_5	A_6	A_7	Column Address
2nd Cycle	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	*L	*L	
3rd Cycle	A_{14}	A_{15}	A_{16}	A_{17}	A_{18}	A_{19}	A_{20}	A_{21}	Row Address; Page Address : A_{14} ~ A_{20}
4th Cycle	A_{22}	A_{23}	A_{24}	A_{25}	A_{26}	A_{27}	A_{28}	A_{29}	Plane Address : A_{21}
5th Cycle	A_{30}	A_{31}	A_{32}	*L	*L	*L	*L	*L	Block Address : A_{22} ~ A_{32}

NOTE :

1) A0 must be set to "Low"
2) Data input/output unit should be 2-byte(16bit).
   Column Address : Starting Address of the Register.
      * When unused address bits shall be set to "Low".
      * The device ignores any additional input of address cycles than required

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2.0 PRODUCT INTRODUCTION

NAND Flash Memory has addresses multiplexed into 8 I/Os. This scheme dramatically reduces pin counts and allows system upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Those are latched on the rising edge of $\overline{WE}$. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. Some commands require one bus cycle. For example, Reset Command, Status Read Command, etc. require just one cycle bus. Some other commands, like page read and block erase and page program, require two cycles: one cycle for setup and the other cycle for execution. Page Read and Page Program need the same five address cycles following the required command input. In Block Erase operation, however, only the three row address cycles are used. Device operations are selected by writing specific commands into the command register. The table below defines the specific commands.

[Table 1] Command Sets

Function	1st Set	2nd Set	Acceptable Command during busy
Read	00h	30h	
Cache Read	31h	-	
Read Start for Last Page Cache Read	3Fh	-	
Read for Copy-Back	00h	35h	
Intelligent Copy-Back Read	00h	3Ah	
Page Program	80h	10h	
Cache Program	80h	15h	
Copy-Back Program	85h	10h	
Intelligent Copy-Back Program	8Ch	15h	
Intelligent Copy-Back Program for Last Page	8Ch	10h	
Block Erase	60h	D0h	
Random Data Input[1]	85h	-	
Random Data Output[1]	05h	E0h	
Two-Plane Read [3]	60h----60h	30h	
Two-Plane Read for Copy-Back[3]	60h----60h	35h	
Two-Plane Intelligent Copy-Back Read	60h----60h	3Ah	
Two-Plane Cache Read[3]	60h----60h	33h	
Two-Plane Random Data Output [1] [3]	00h----05h	E0h	
Two-Plane Page Program[2]	80h----11h	81h----10h	
Two-Plane Copy-Back Program[2]	85h----11h	81h----10h	
Two-Plane Intelligent Copy-Back Program	8Ch----11h	8Ch----15h	
Two-Plane Cache Program[2]	80h----11h	81h----15h	
Two-Plane Intelligent Copy-Back Program for Last Page	8Ch----11h	8Ch----10h	
Two-Plane Block Erase	60h----60h	D0h	
Read ID	90h	-	
Device Identification Table Read	ECh	-	
Read Status	70h	-	O
Read chip#0 status	F1h	-	O
Read chip#1 status	F2h	-	O
Set Feature	EFh	-	
Reset	FFh	-	O

NOTE :

1) Random Data Input/Output can be executed in a page.

2) Any command between 11h and 80h/81h/85h is prohibited except 70h/F1h/F2h and FFh.

3) Two-Plane Random Data out must be used after Two-Plane Read or Two-Plane Cache Read operation

CAUTION :
Any undefined command inputs are prohibited except for above command set of Table 1 .

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2.1 Absolute Maximum DC Rating

Stresses greater than those listing in Table 2 may cause permanent damage to the device. This is a stress rating only. Operation beyond the operating conditions specified in Table 2 is not recommended. Extended exposure beyond these conditions may affect device reliability.

[Table 2] Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V_{CC}	-0.6 to +4.6	V
	V_{CCQ}	-0.6 to +4.6	
	V_{IN}	-0.6 to VccQ + 0.3(<4.6)	
	$V_{I/O}$		
Storage Temperature	T_{STG}	-65 to +100	°C

NOTE :
1) Minimum DC voltage is -0.6V on input/output pins at 3.3VccQ. During transitions, this level may undershoot to -2.0V for periods <30ns.
   Maximum DC voltage on input/output pins is 4.6V at 3.3VccQ which, during transitions, may overshoot to VccQ+2.0V for periods <20ns.
2) Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions
   as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2.2 Recommended Operating Conditions

(Voltage reference to GND, K9XXG08U0B-SCB0:T_A=0 to 70°C[1])

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC}	2.7	3.3	3.6	V
Ground Voltage	V_{SS}	0	0	0	V
Supply Voltage for I/O signaling (3.3V)	V_{CCQ}	2.7	3.3	3.6	V
Ground Voltage for I/O signaling	V_{SSQ}	0	0	0	V

NOTE :
1) Data retention is not guaranteed on out of operating condition temperature.

2.3 DC And Operating Characteristics(Recommended operating conditions otherwise noted.)

[Table 3] DC & Operating Characteristics for VccQ=3.3V

Parameter	Symbol	Test Conditions	2-Plane			Unit
			Min	Typ	Max	
Page Read Operation Current	I_{CC1}	-	-	-	45	mA
Page Program Operation Current	I_{CC2}	-	-	-	45	
Erase Operation Current	I_{CC3}	-	-	-	45	
I/O Burst Read Current	I_{CC4R}	C_{LOAD}=0pF (I_{OUT}=0mA) $\overline{CE}$=V_{IL}, Half data switching tRC=10ns(100Mhz)	-	-	-	
	I_{CCQ4R}		-	-	-	
I/O Burst Write Current	I_{CC4W}	$\overline{CE}$=V_{IL}, Half data switching	-	-	-	
	I_{CCQ4W}		-	-	-	
Bus Idle Current	I_{CC5}	-	-	-	-	
Stand-by Current(CMOS)	I_{SB}[3]	$\overline{CE}$=VccQ-0.2, $\overline{WP}$=0V/VccQ	-	-	-	
Input Leakage Current	I_{LI}[4]	V_{IN}=0 to VccQ(max)	-	-	±10	µA
Output Leakage Current	I_{LO}[4]	V_{OUT}=0 to VccQ(max)	-	-	±10	
Output High Voltage Level	V_{OH}	I_{OH}=-400µA	2.4	-	-	V
Output Low Voltage Level	V_{OL}	I_{OL}= 2.1mA	-	-	0.4	
Output Low Current(R/$\overline{B}$)	I_{OL}(R/$\overline{B}$)	V_{OL}=0.4V	8	10	-	mA

NOTE :
1) Typical value is measured at Vcc=3.3V, T_A=25°C. Not 100% tested.
2) VOH and VOL should be available on these two conditions; Output Strength is nominal and VccQ=3.3V, Rpd/Rpu are all VccQx0.5. If the driver strength settings are
   supported, Table 14 shall be used to derive the output driver impedence values.

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2.4 Valid Block

Parameter	Symbol	Min	Typ.	Max	Unit
K9GBG08U0B	N_{VB}	3,994	-	4,096	Blocks
K9LCG08U0B		7,988		8,192	

NOTE :
1) The device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits which cause status failure during program and erase operation. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of initial invalid blocks.
2) The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment.
3) The number of valid blocks is on the basis of single plane operations, and this may be decreased with two plane operations.

2.5 AC Test Condition

(K9XXG08U0B-SCB0:T_A=0 to 70°C, VCC=2.7V~3.6V, unless otherwise noted)

Parameter	K9XXG08U0B
Input Pulse Levels	V_{IL} to V_{IH}
Input Rise and Fall Times	1.0V/ns
Input and Output Timing Levels	VccQ/2
Output Load	CL= 5pF

2.6 Capacitance(T_A=25°C, VCC=3.3V, f=1MHz)

Item	Symbol	Test Condition	K9XXG08U0B		Unit
			Min	Max	
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	8	pF
	$C_{I/O(W)}$*		-	5	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	8	pF
	$C_{IN(W)}$*		-	5	pF

NOTE :
1) Capacitance is periodically sampled and not 100% tested.
2) CI/O(W) and CIN(W) are tested at wafer level.

2.7 Mode Selection

CLE	ALE	CE	WE	RE	WP	Mode	
H	L	L	⎍	H	X	Read Mode	Command Input
L	H	L	⎍	H	X		Address Input(5clock)
H	L	L	⎍	H	H	Write Mode	Command Input
L	H	L	⎍	H	H		Address Input(5clock)
L	L	L	H	H	H	Data Input	
L	L	L	H	⎍	X	Data Output	
X	X	X	X	H	X	During Read(Busy)	
X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X[1]	X	X	X	L	Write Protect	
X	X	H	X	X	0V/Vcc[2]	Stand-by	

NOTE :
1) X can be VIL or VIH.
2) WP should be biased to CMOS high or CMOS low for standby.

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2.8 Program / Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data Transfer from Flash array to Register	tR	-	-	80	μs
Program Time	tPROG	-	1.3	5	ms
Dummy Busy Time for Two-Plane setting	tDBSY	-	0.5	1	μs
Dummy Busy Time for Cache Program	tCBSY	-	-	tPROG	ms
Dummy Busy Time for Intelligent Copy-Back Program	tCBSY2	-	-	tR	μs
Cache Busy in Read Cache	t_{DCBSYR}	-	-	tR	μs
Dummy Busy Time for Intelligent Copy-Back Read	$t_{DCBSYR2}$	-	-	tPROG	ms
Number of Partial Program Cycles in the Same Page	Nop	-	-	1	cycle
Block Erase Time	tBERS	-	5	10	ms

NOTE :
1) Typical program time is measured at Vcc=3.3V, TA=25°C. Not 100% tested.
2) Typical Program time is defined as the time within which more than 50% of the whole pages are programed at 3.3V Vcc and 25°C temperature.
3) Within a same block, program time(tPROG) of page group A is faster than that of page group B. Typical tPROG is the average program time of the page group A and B.
   Page Group A: Page 0, 1, 3, 5, 7, 9, 11, ... ,115, 117, 119, 121, 123, 125
   Page Group B: Page 2, 4, 6, 8, 10, 12, ... , 118, 120, 122, 124, 126, 127
4) tCBSY depends on the timing between internal programming time and data in time.

2.9 AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	Min	Max	Unit
CLE Setup Time	tCLS[1]	12	-	ns
CLE Hold Time	tCLH	5	-	ns
CE Setup Time	tCS[1]	20	-	ns
CE Hold Time	tCH	5	-	ns
RE Set up time	tCRES	10	-	ns
WE Pulse Width	tWP	11	-	ns
ALE Setup Time	tALS[1]	12	-	ns
ALE Hold Time	tALH	5	-	ns
Data Setup Time	tDS[1]	12	-	ns
Data Hold Time	tDH	5	-	ns
Write Cycle Time	tWC	25	-	ns
WE High Hold Time	tWH	11	-	ns
Address to Data Loading Time	tADL[2]	300	-	ns

NOTE :
1) The transition of the corresponding control pins must occur only once while WE is held low
2) tADL is the time from the WE rising edge of final address cycle to the WE rising edge of first data cycle

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2.10 AC Characteristics for Operation

Parameter	Symbol	Min	Max	Unit
ALE to RE Delay	tAR	10	-	ns
CLE to RE Delay	tCLR	10	-	ns
Command Write cycle to Address Write cycle Time for Random data input	tCWAW	300	-	ns
Ready to RE Low	tRR	20	-	ns
RE Pulse Width	tRP	11	-	ns
Read Cycle Time	tRC	25	-	ns
RE Access Time	tREA	-	20	ns
RE High to Output hold	tRHOH	15		ns
CE Access Time	tCEA	-	25	ns
CE Hold Time	tCH	5	-	ns
RE High to Output Hi-Z	tRHZ	-	100	ns
CE High to Output Hi-Z	tCHZ	-	30	ns
CLE to RE Low	tCLR	10	-	ns
RE Set up time	tCRES	10	-	ns
CE Setup Time	tCS	25	-	ns
CE High to ALE, CLE or WE Don't Care	tCSD	10	-	ns
Data Hold Time	tDH	0.9	-	ns
Data Setup Time	tDS	0.9	-	ns
RE Low to Output Hold	tRLOH	5	-	ns
RE High Hold Time	tREH	11	-	ns
Output Hi-Z to RE Low	tIR	0	-	ns
RE High to WE Low	tRHW	100	-	ns
Device Resetting Time(Read/Program/Erase)	tRST	-	10/30/200(1)	μs
Busy time for Set Feature and Get Feature	tFEAT	-	1	μs
Cache Busy in Read Cache (following 31h and 3Fh)	tDCBSYR	-	200(2)	μs
Dummy Busy Time for Intelligent Copy-Back Read	tDCBSYR2	-	5	ms
WE High to Busy	tWB	-	100	ns
Write Cycle Time	tWC	25	-	ns
WE High pulse width	tWH	11	-	ns
WE High to RE Low	tWHR	120	-	ns
WE High to RE Low for Random data out	tWHR2	300	-	ns
WE Low pulse Width	tWP	11	-	ns
WP High/Low to WE low	tWW	100ns	-	ns

NOTE :
1) If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 10μs.
2) 200us is applied for the tR maximum value.

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3.0 NAND FLASH TECHNICAL NOTES

3.1 Initial Invalid Block(s)

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by Samsung. The information regarding the initial invalid block(s) is called the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment.

3.2 Identifying Initial Invalid Block(s)

All device locations are erased(FFh) except locations where the initial invalid block(s) information is written prior to shipping. The initial invalid block(s) status is defined by the 1st byte in the spare area. Samsung makes sure that the first or the last page of every initial invalid block has non-FFh data at the both column address of 0 and 8,192.The initial invalid block information is also erasable in most cases, and it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the initial invalid block(s) based on the initial invalid block information and create the initial invalid block table via the following suggested flow chart. Any intentional erasure of the initial invalid block information is prohibited.
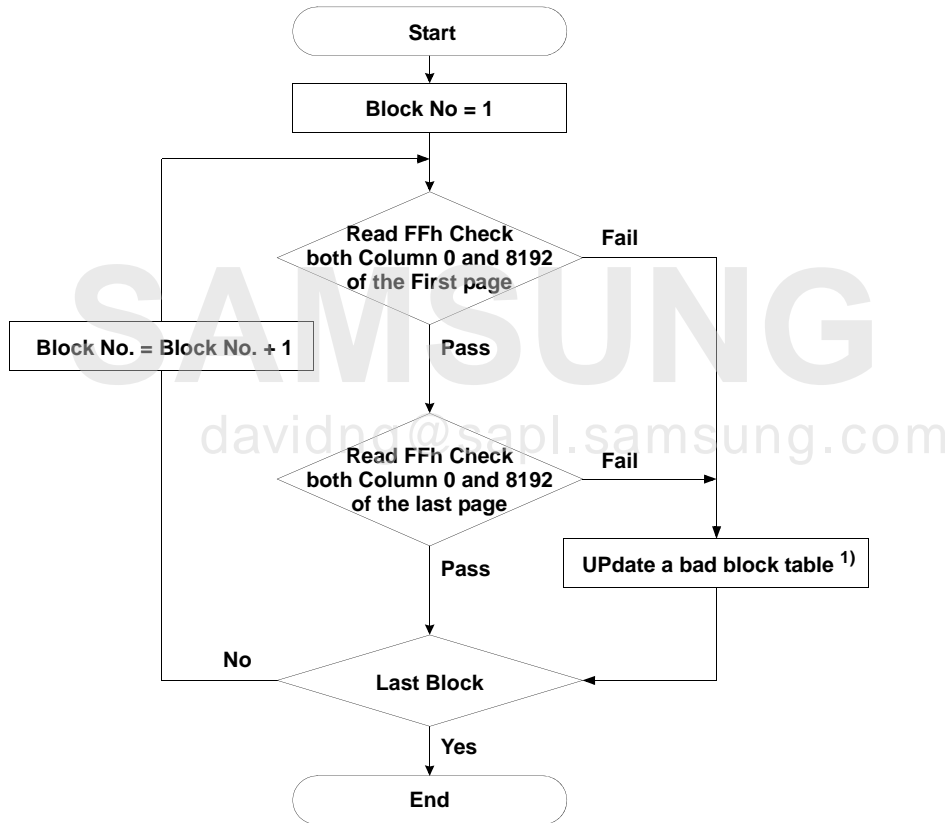
Flow chart to create initial invalid block table.

NOTE :
1) No erase operation is allowed to detected bad blocks.

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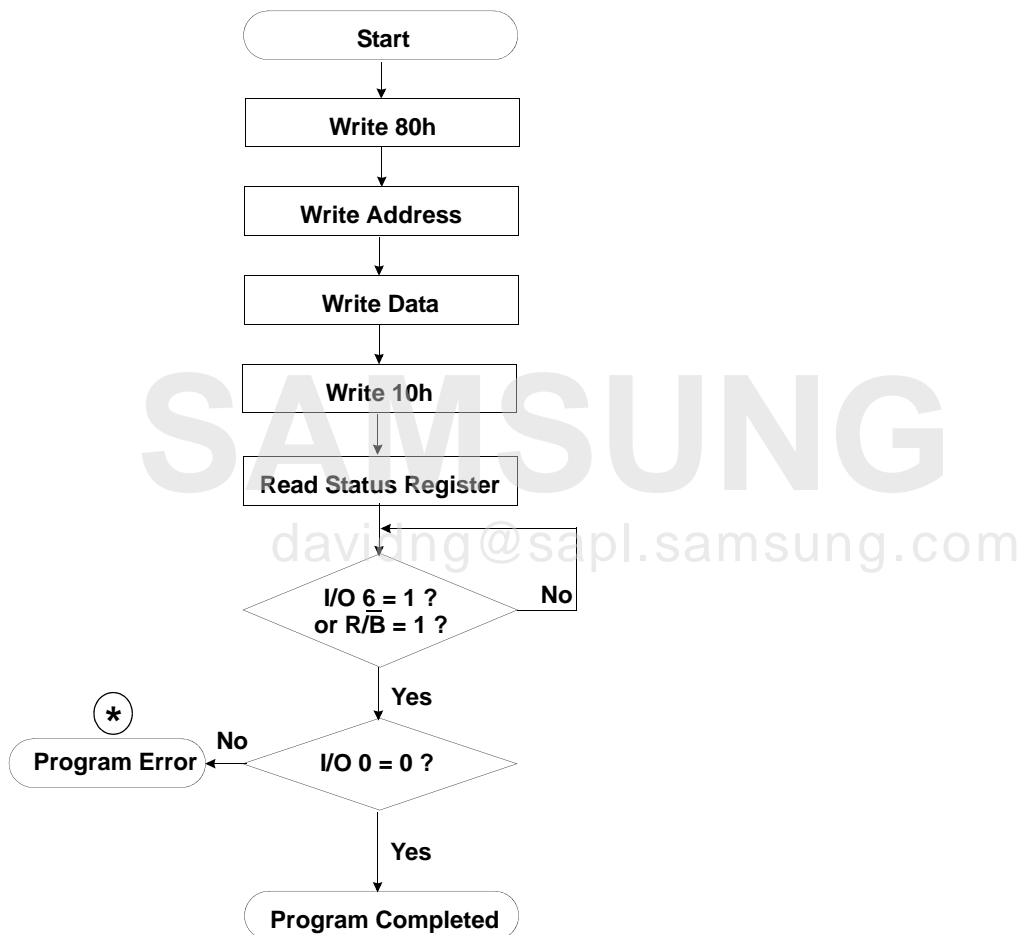
datasheet

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3.3 Error In Write or Read Operation

Within its life time, additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data. Block replacement should be done upon erase or program error.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase --> Block Replacement
	Program Failure	Status Read after Program --> Block Replacement
Read	Up to 40-Bits Failure	Verify ECC -> ECC Correction

ECC : Error correcting code such as BCH code.
Example) 40 bit correction / 1KB

Program Flow Chart


```
Start
  ↓
Write 80h
  ↓
Write Address
  ↓
Write Data
  ↓
Write 10h
  ↓
Read Status Register
  ↓
I/O 6 = 1 ? or R/B = 1 ?  -- No (loop back)
  ↓ Yes
I/O 0 = 0 ?  -- No --> * Program Error
  ↓ Yes
Program Completed
```
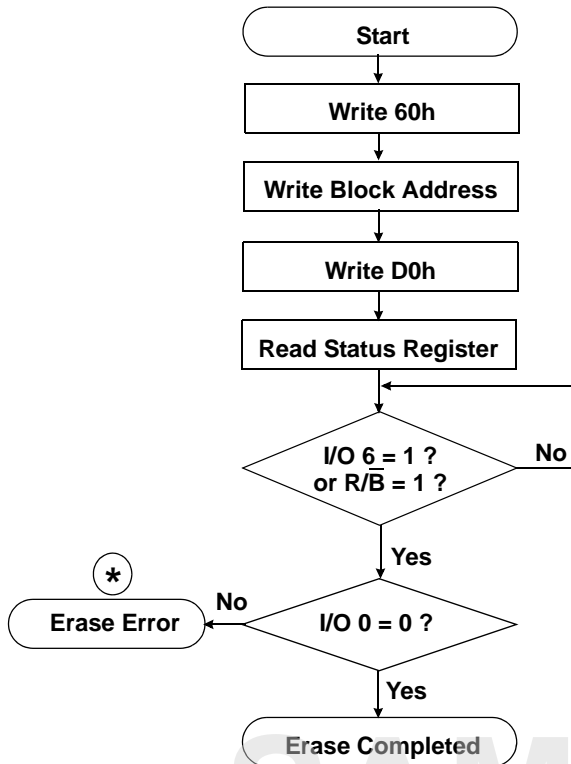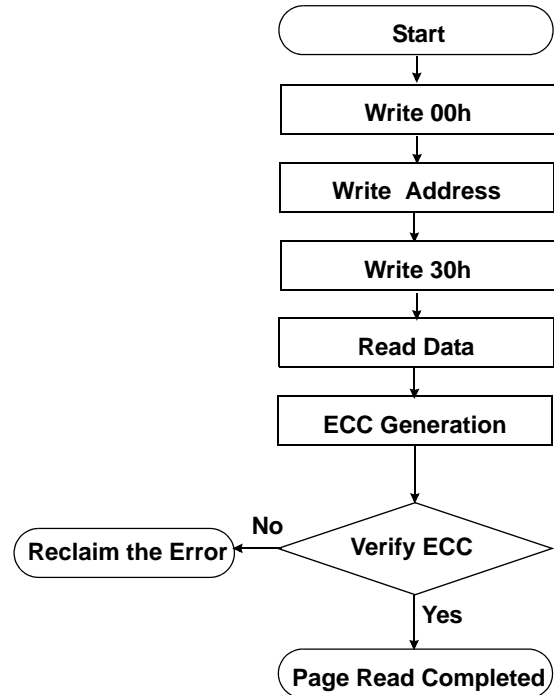
(*) : If program operation results in an error, map out the block including the page in error and copy the target data to another block.

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NAND Flash Technical Notes *(Continued)*

Erase Flow Chart

Start
↓
Write 60h
↓
Write Block Address
↓
Write D0h
↓
Read Status Register
↓
I/O 6 = 1 ?
or R/B = 1 ? → **No**
↓ **Yes**

I/O 0 = 0 ? → **No** → * Erase Error
↓ **Yes**

Erase Completed

(*) : **If erase operation results in an error, map out the failing block and replace it with another block.**

Read Flow Chart

Start
↓
Write 00h
↓
Write Address
↓
Write 30h
↓
Read Data
↓
ECC Generation
↓
Verify ECC → **No** → Reclaim the Error
↓ **Yes**

Page Read Completed

Block Replacement

Block A

1st
~
(n-1)th
nth → an error occurs. ①
(page)

Buffer memory of the controller.

Block B

1st
~
(n-1)th
nth → ②
(page)
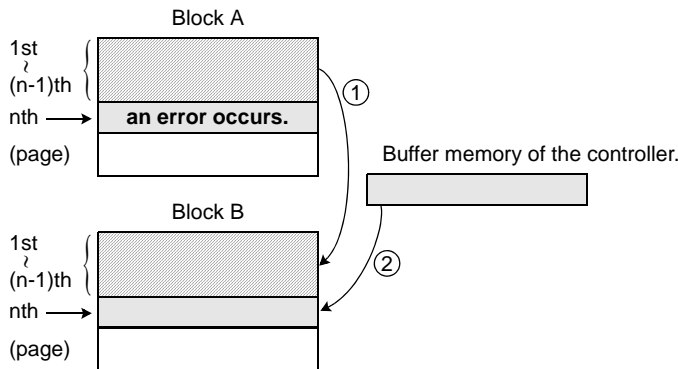
* Step1
When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step2
Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
* Step3
Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'.
* Step4
Do not erase or program to Block 'A' by creating an 'invalid block' table or other appropriate scheme.

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3.4 Addressing For Program Operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) pages of the block. Random page address programming is prohibited. In this case, the definition of LSB page is the LSB among the pages to be programmed. Therefore, LSB doesn't need to be page 0.

A page in 'group A' must be programmed before the program operation for a page in 'group B' is performed

Page 127	(127)
	:
Page 63	(63)
	:
Page 2	(3)
Page 1	(2)
Page 0	(1)

Data register

From the LSB page to MSB page

DATA IN: Data (1) ⟶ Data (128)

Page 127	(127)
	:
Page 63	(1)
	:
Page 2	(3)
Page 1	(32)
Page 0	(2)

Data register

Random page program (Not allowed)

DATA IN: Data (1) ⟶ Data (128)

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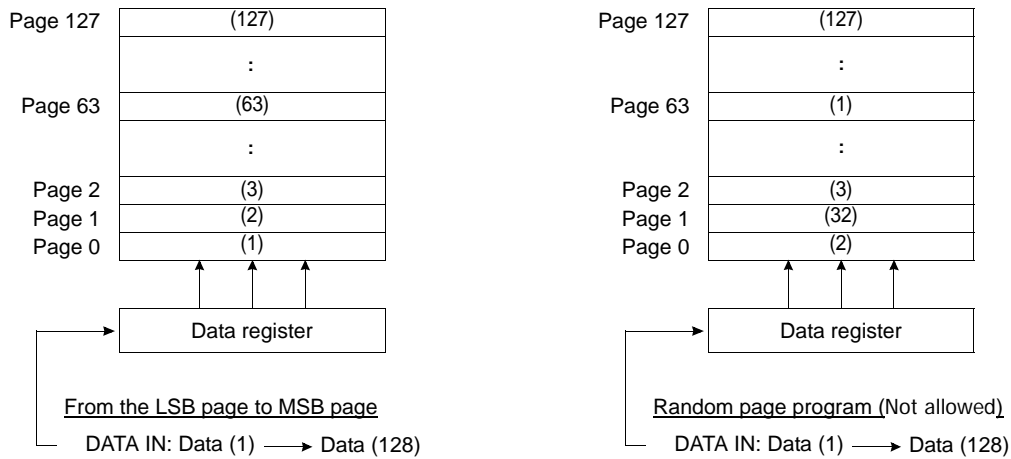
Paired Page Address Information

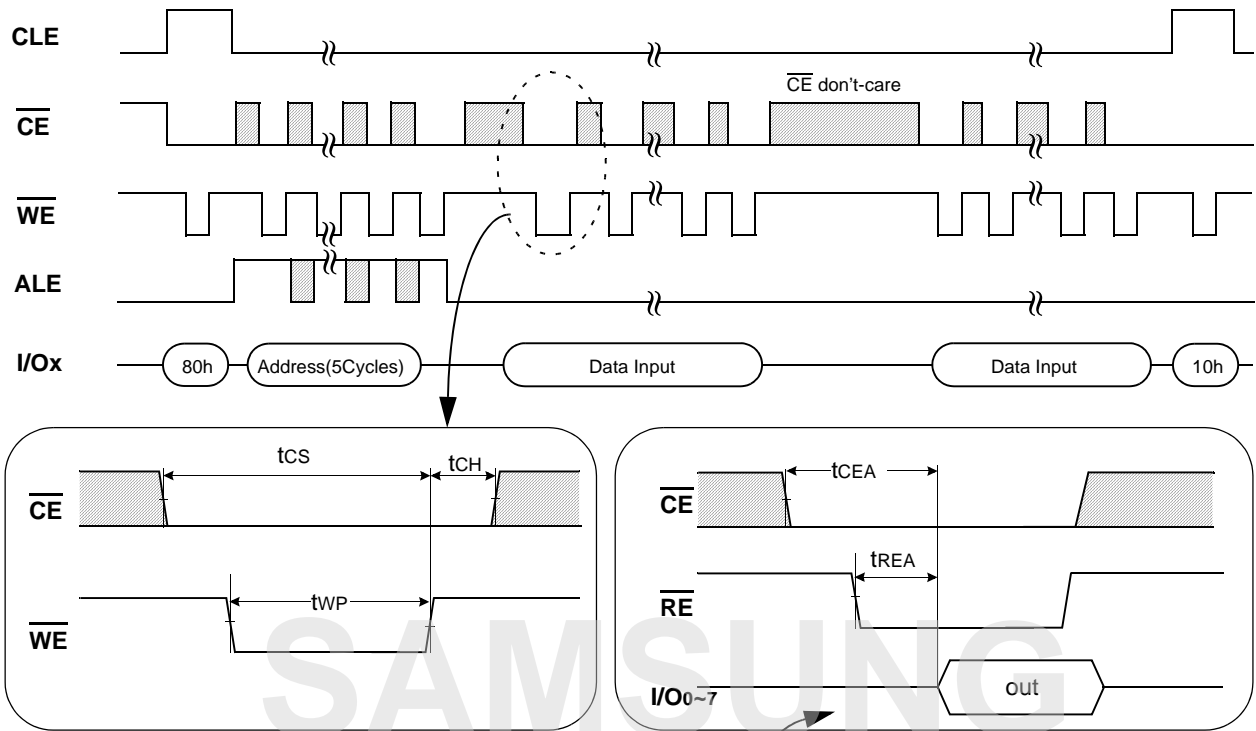| Paired Page Address(1/2)		Paired Page Address(2/2)	
Group A	Group B	Group A	Group B
00h	02h	3Fh	42h
01h	04h	41h	44h
03h	06h	43h	46h
05h	08h	45h	48h
07h	0Ah	47h	4Ah
09h	0Ch	49h	4Ch
0Bh	0Eh	4Bh	4Eh
0Dh	10h	4Dh	50h
0Fh	12h	4Fh	52h
11h	14h	51h	54h
13h	16h	53h	56h
15h	18h	55h	58h
17h	1Ah	57h	5Ah
19h	1Ch	59h	5Ch
1Bh	1Eh	5Bh	5Eh
1Dh	20h	5Dh	60h
1Fh	22h	5Fh	62h
21h	24h	61h	64h
23h	26h	63h	66h
25h	28h	65h	68h
27h	2Ah	67h	6Ah
29h	2Ch	69h	6Ch
2Bh	2Eh	6Bh	6Eh
2Dh	30h	6Dh	70h
2Fh	32h	6Fh	72h
31h	34h	71h	74h
33h	36h	73h	76h
35h	38h	75h	78h
37h	3Ah	77h	7Ah
39h	3Ch	79h	7Ch
3Bh	3Eh	7Bh	7Eh
3Dh	40h	7Dh	7Fh

NOTE :
When program operation is abnormally aborted (ex. power-down, reset), not only page data under program but also paired page data may be damaged.

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3.5 System Interface Using $\overline{CE}$ don't-care.

For an easier system interface, $\overline{CE}$ may be inactive during the data-loading or serial access as shown below. The internal 8,704byte data registers are utilized as separate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of μ-seconds, de-activating $\overline{CE}$ during the data-loading and serial access would provide significant savings in power consumption.

Program Operation with $\overline{CE}$ don't-care
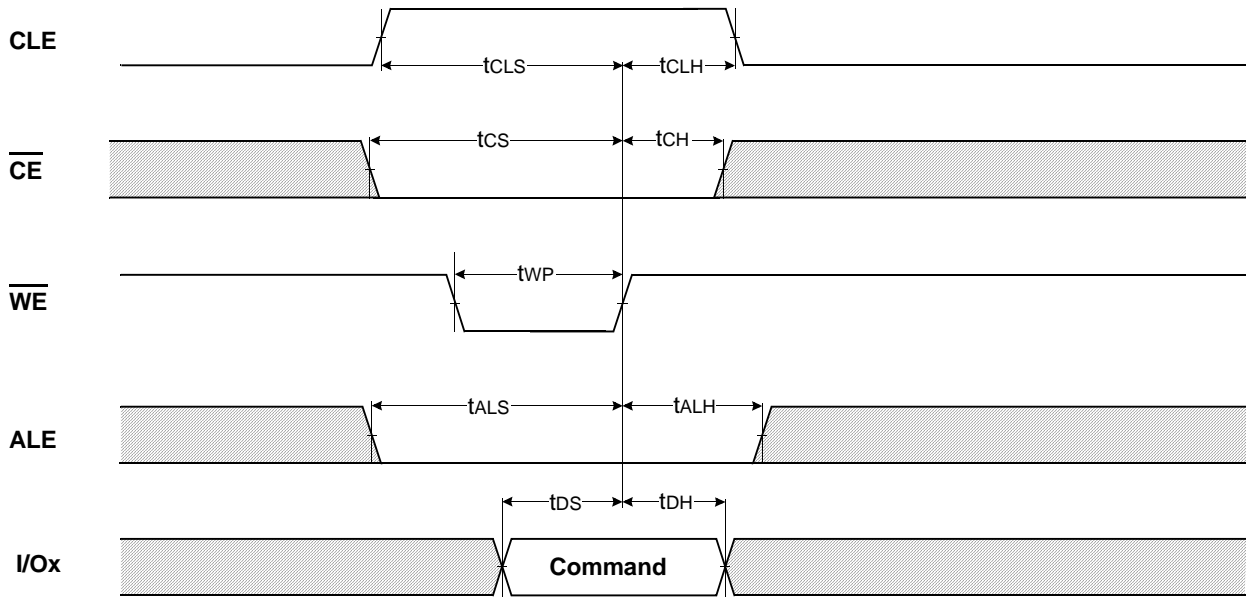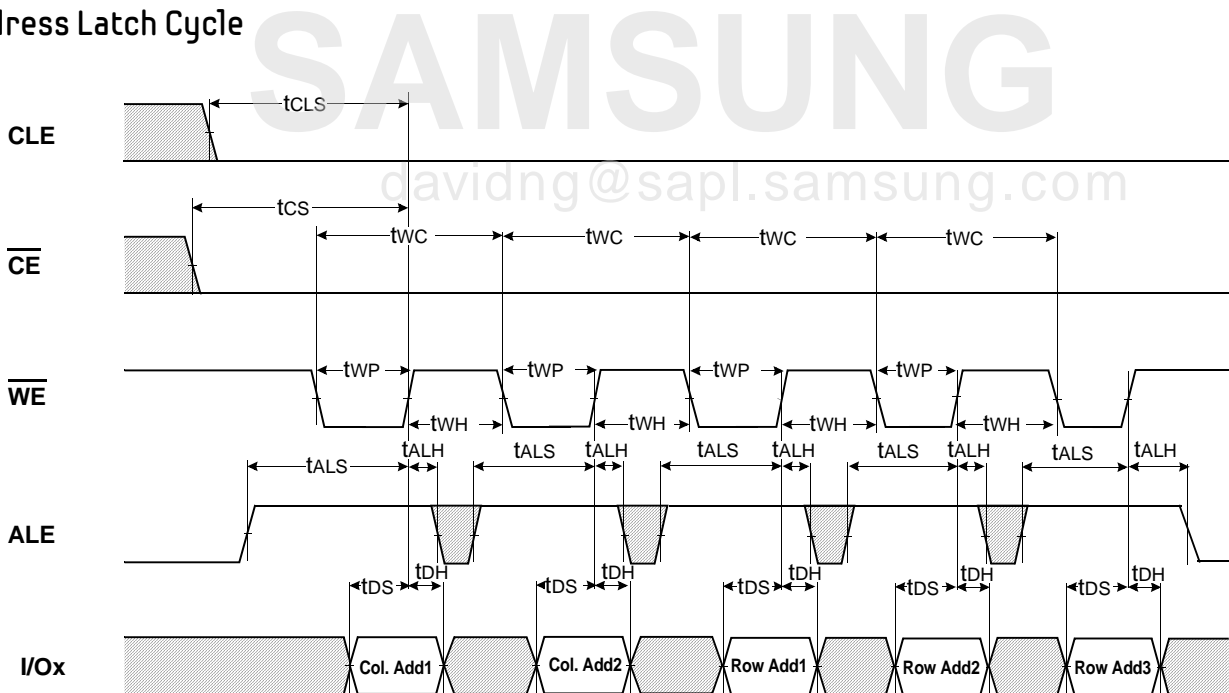

Read Operation with $\overline{CE}$ don't-care

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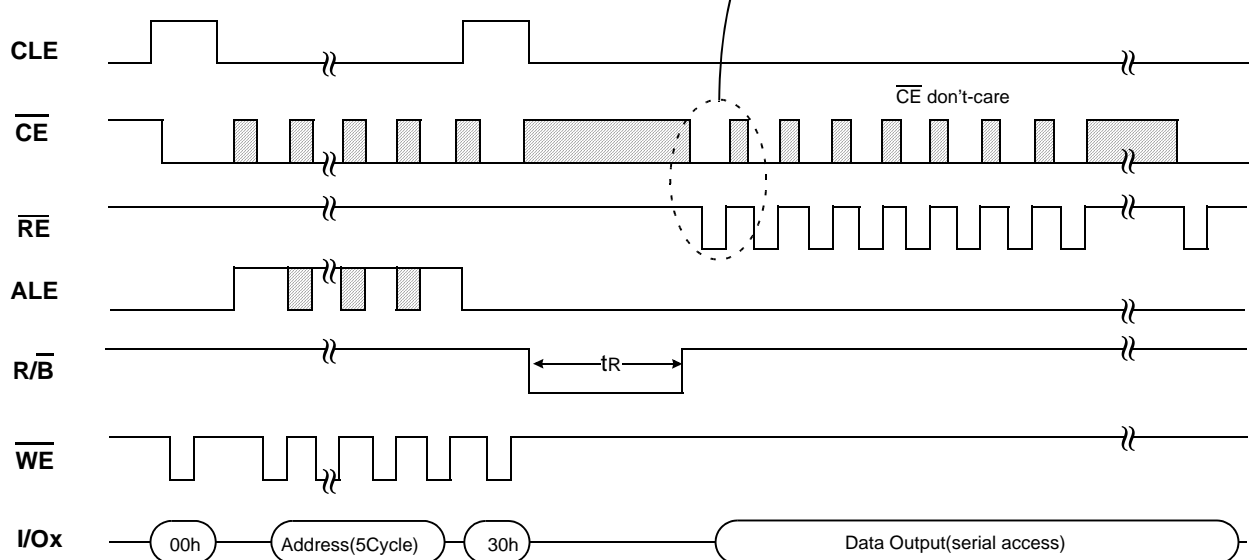
4.0 TIMING DIAGRAMS

4.1 Command Latch Cycle

4.2 Address Latch Cycle

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4.3 Input Data Latch Cycle
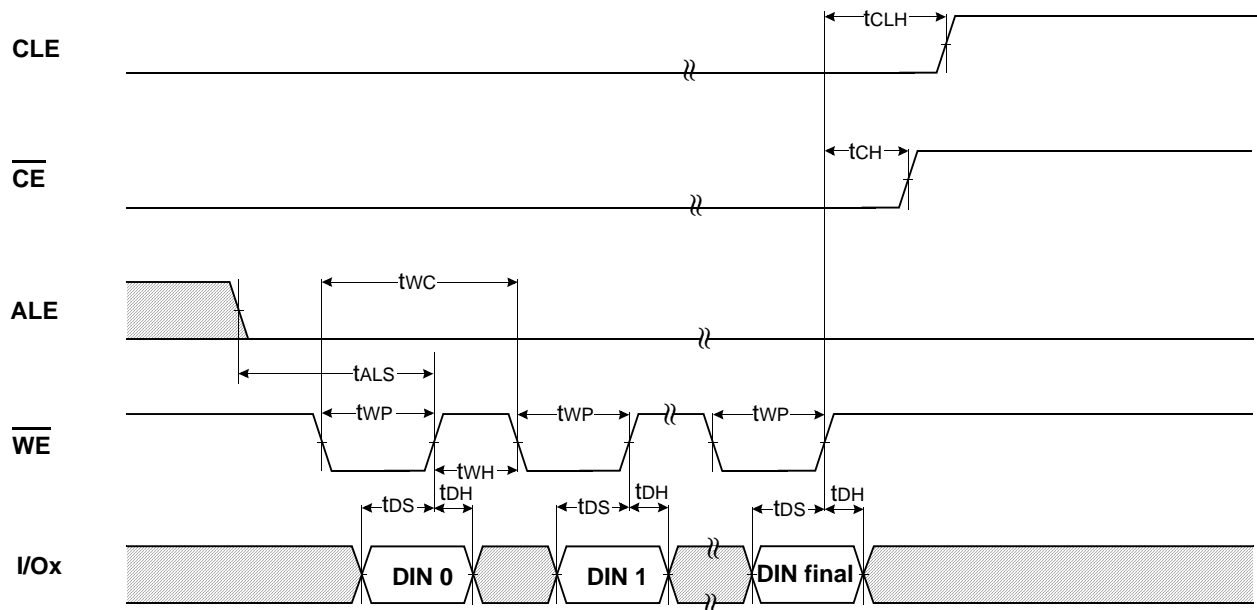
4.4 * Serial Access Cycle after Read(CLE=L, $\overline{WE}$=H, ALE=L)
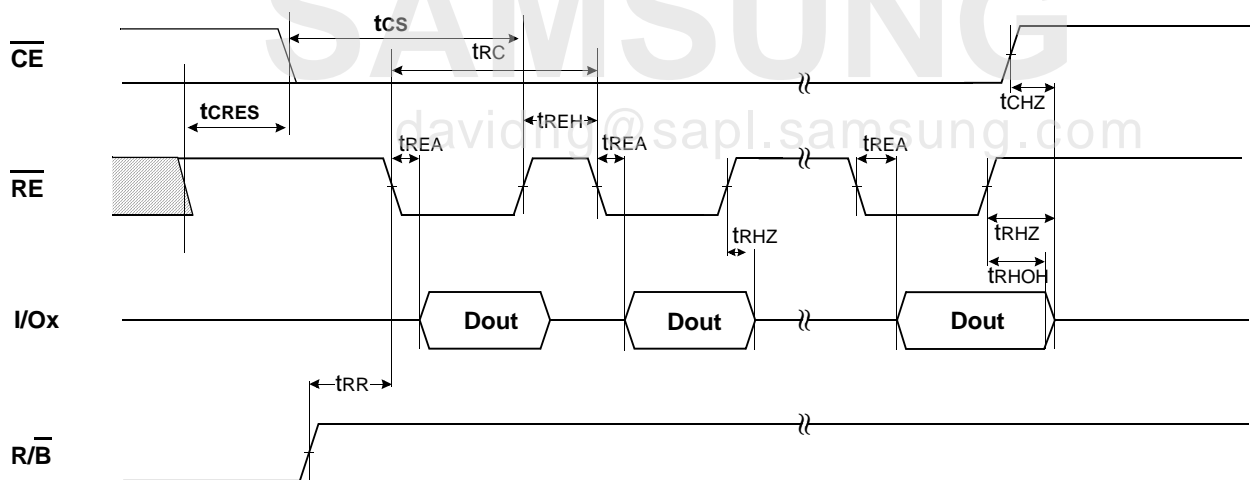
NOTE :
1) Transition is measured at ±200mV from steady state voltage with load.
   This parameter is sampled and not 100% tested.
2) tRLOH is valid when frequency is higher than 20MHz.
   tRHOH starts to be valid when frequency is lower than 20MHz.

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4.5 Serial Access Cycle after Read (EDO Type, CLE=L, WE=H, ALE=L)
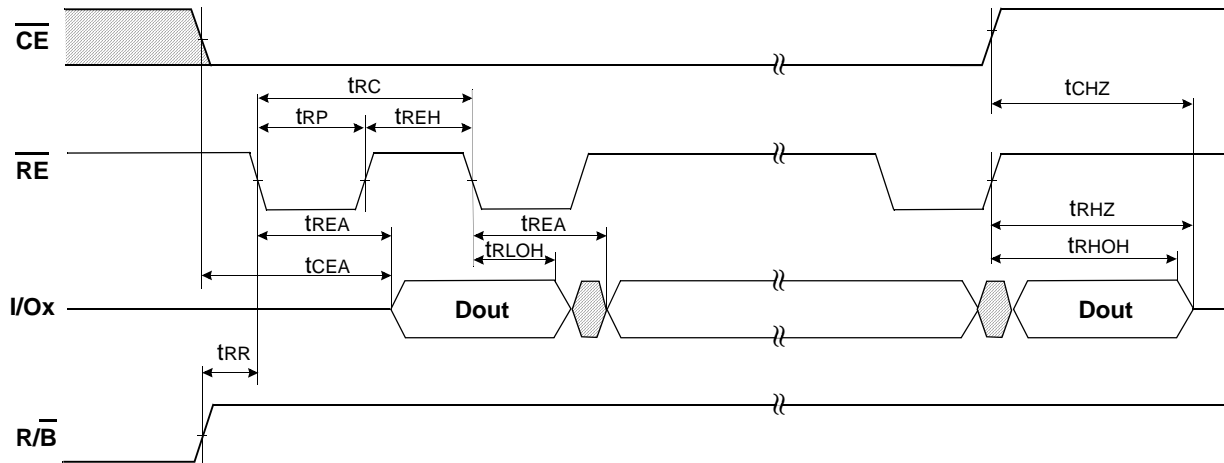
NOTE :
1) Transition is measured at ±200mV from steady state voltage with load.
   This parameter is sampled and not 100% tested.
2) tRLOH is valid when frequency is higher than 20MHz.
   tRHOH starts to be valid when frequency is lower than 20MHz.

4.6 Status Read Cycle

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4.7 Read Operation

4.8 Read Operation (Intercepted by $\overline{CE}$)

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4.9 Random Data Output In a Page

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4.10 Cache Read Operation

NOTE :
1) The column address will be reset to 0 by the 31h and 3Fh command input.
2) Cache Read operation is available only within a block.

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4.11 Two-Plane Page Read Operation with Two-Plane Random Data Out

CLE

CE

WE

ALE

RE

I/Ox

R/B

tWC

tWC

tWB

tR

60h | Row Add1 | Row Add2 | Row Add3

Row Address

60h | Row Add1 | Row Add2 | Row Add3 | 30h

Row Address

page address : Page M
plane address: Fixed 'Low'
block address : Block N

page address : Page M
plane address: Fixed 'High'
block address : Block N

Busy

1

CLE

CE

WE

ALE

RE

I/Ox

R/B

tCLR

tWC

tWHR2

tREA

tRC

00h | Col. Add1 | Col. Add2 | Row Add1 | Row Add2 | Row Add3

Column Address | Row Address

05h | Col. Add1 | Col. Add2 | E0h

Column Address

Dout N | Dout N+1

column address : Valid

column address : Valid

column address : Fixed 'Low'
page address : Page M
plane address : Fixed 'Low'
block address : Block N

1

2

CLE

CE

WE

ALE

RE

I/Ox

R/B

tCLR

tCLR

tWC

tWHR2

tWHR2

tREA

tRHW

tREA

tRC

tRC

E0h | Dout N | Dout N+1 | 00h | Col. Add1 | Col. Add2 | Row Add1 | Row Add2 | Row Add3 | 05h | Col. Add1 | Col. Add2 | E0h | Dout M | Dout M+1

Column Address | Row Address

Column Address

column address: Fixed 'Low'
page address   Page M
plane address : Fixed 'High'
block address : Block N

column address : Valid

2

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4.12 Two-Plane Cache Read Operation with Two-Plane Random Data Out (1/2)

CLE

CE

WE   tWC   tWC

ALE   tWB

RE   tR

I/Ox   60h Row Add1 Row Add2 Row Add3   60h Row Add1 Row Add2 Row Add3 33h
         Row Address   Row Address

R/B   page address : Page M   page address : Page M   Busy
       plane address: Fixed 'Low'   plane address: Fixed 'High'
       block address : Block N   block address : Block N   1

CLE

CE   tCLR

WE   tWC   tWHR2

ALE   tDCBSYR   tREA

RE   tWB   tRC

I/Ox   31h   00h Col. Add1 Col. Add2 Row Add1 Row Add2 Row Add3   05h Col. Add1 Col. Add2 E0h   Dout N Dout N+1
              Column Address Row Address   Column Address

R/B   column address : Fixed 'Low'   column address : Valid
       page address   : Page M
       plane address : Fixed 'Low'
       block address : Block N   2

1   **Max. 127 times repeatable**

CLE

CE   tCLR

WE   tWC   tWHR2   tWC

ALE   tDCBSYR   tREA

RE   tRC   tWB

I/Ox   Dout N+1 00h Col. Add1 Col. Add2 Row Add1 Row Add2 Row Add3 05h Col. Add1 Col. Add2 E0h Dout M Dout M+1 3Fh 00h Col. Add1 Col. Add2 Row Add1 Row Add2 Row Add3
                  Column Address Row Address   Column Address   Column Address Row Address

R/B   column address: Fixed 'Low'   column address : Valid   column address : Fixed 'Low'
       page address   Page M   page address   : Page M+n
       plane address : Fixed 'High'   plane address : Fixed 'Low'
       block address : Block N   **Max. 127 times repeatable**   block address : Block N
2   3

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4.13 Two-Plane Cache Read Operation with Two-Plane Random Data Out (2/2)

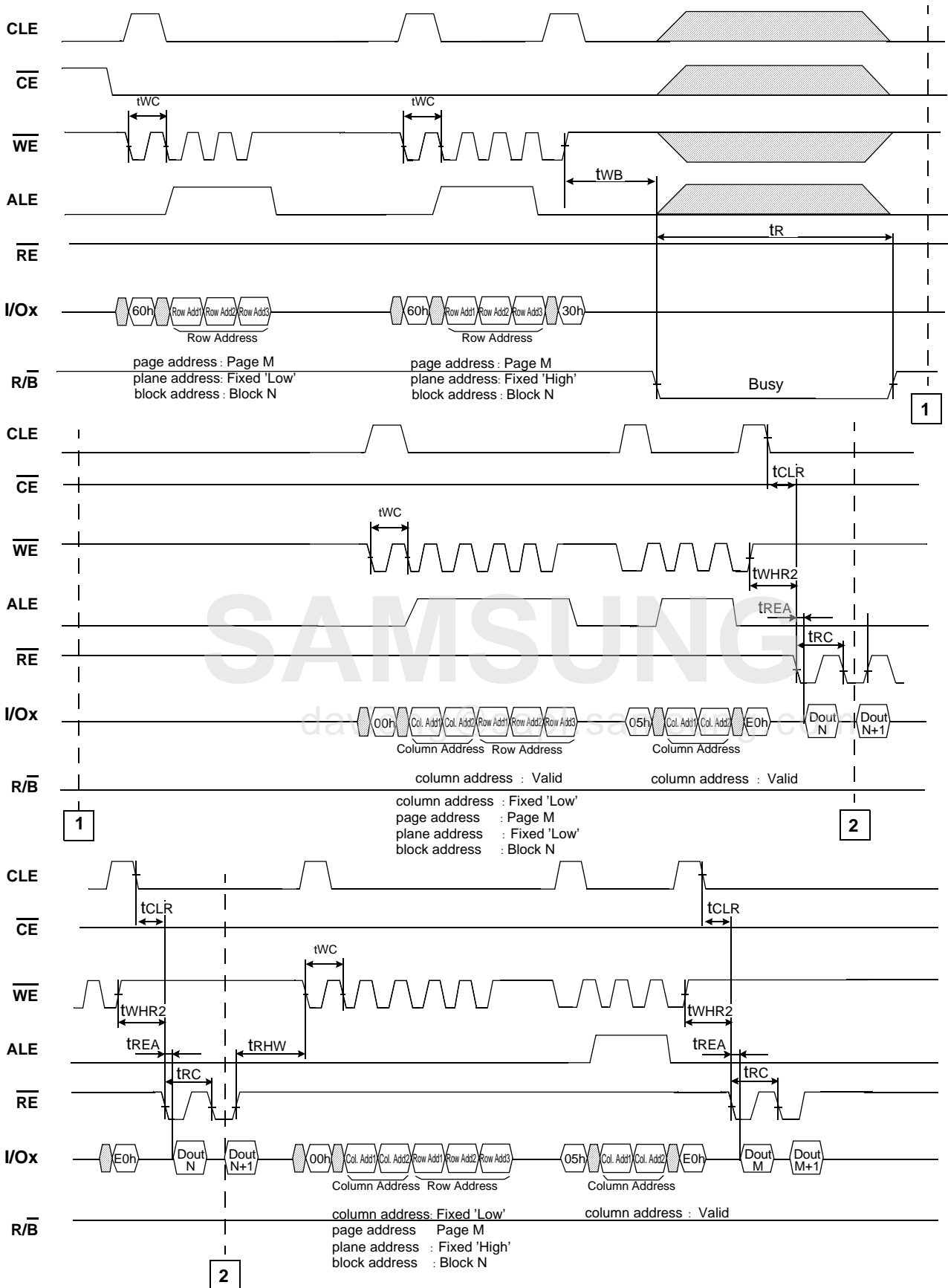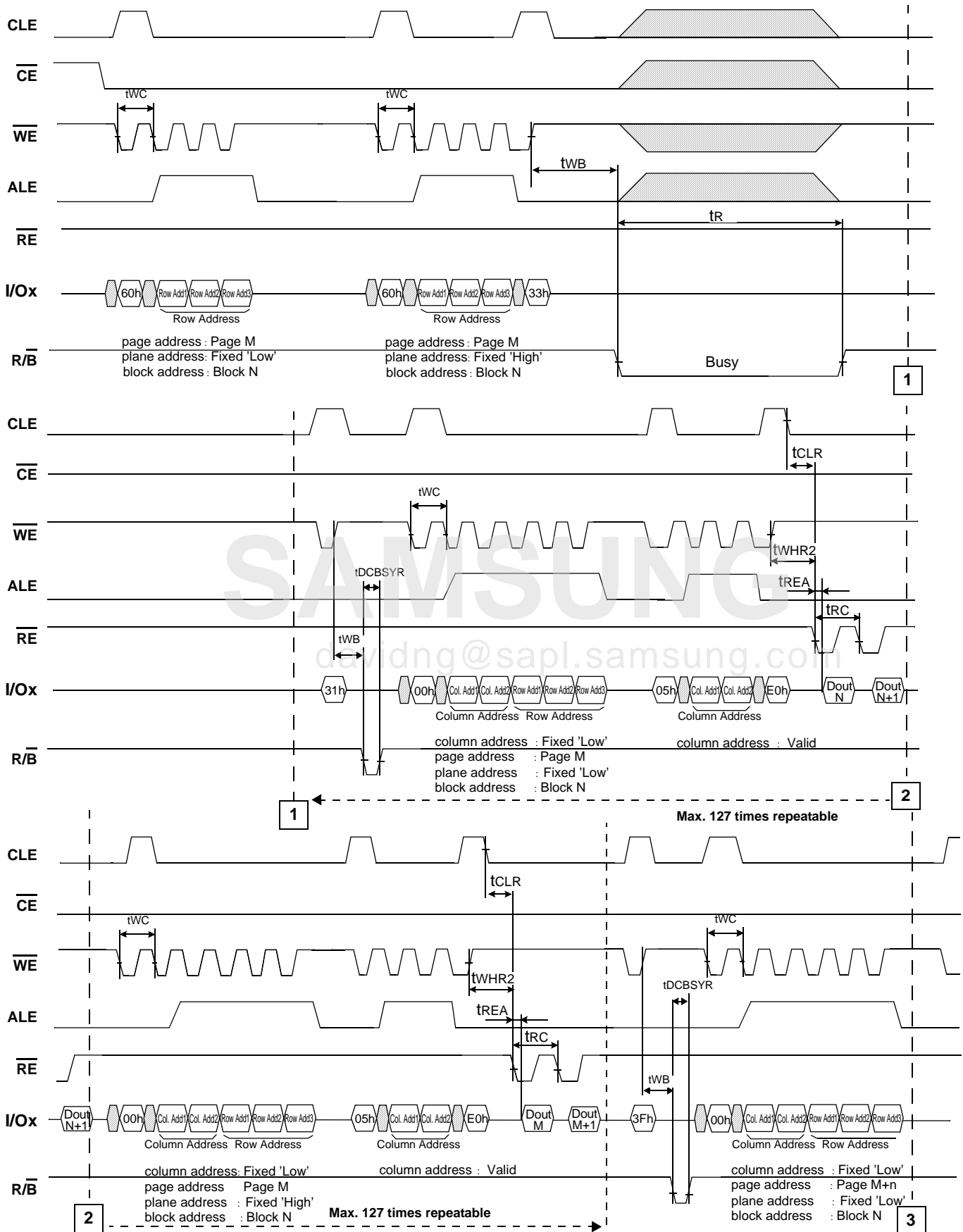**NOTE :**
1) The column address will be reset to 0 by the 3Fh command input.
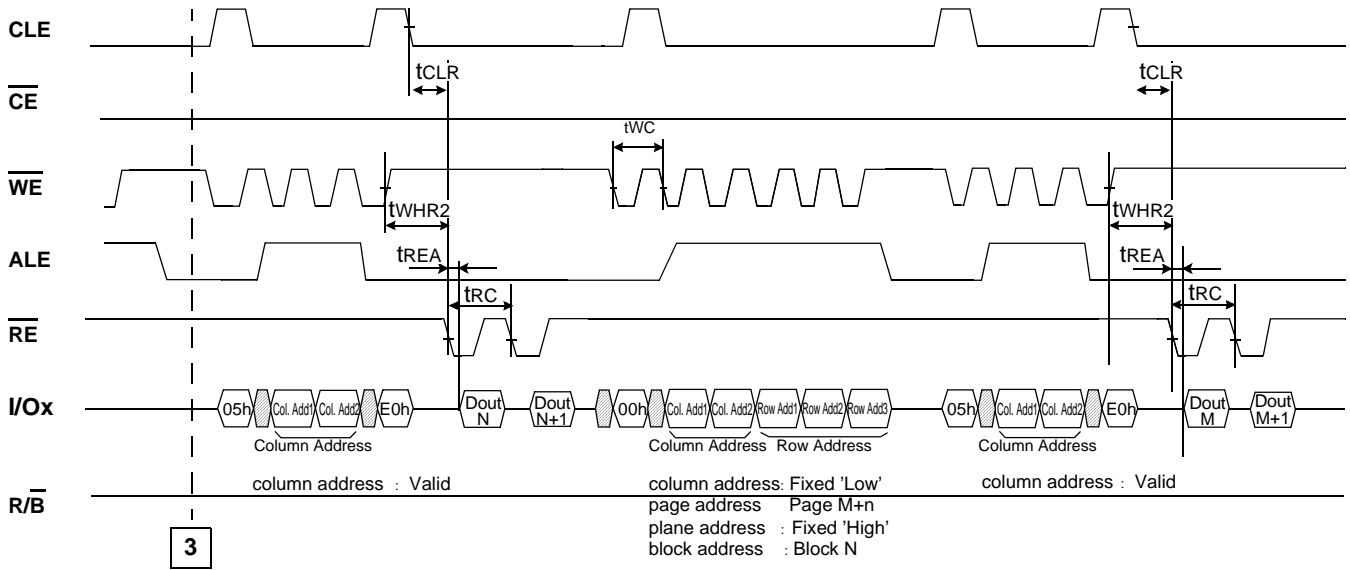2) Cache Read operation is available only within a block.
3) Make sure to terminate the operation with 3Fh command. If the operation is terminated by 31h command, monitor I/O 6 (Ready/Busy) by issuing Status Read Command (70h/F1h/F2h) and make sure the previous page read operation is completed. If the page read operation is completed, issue FFh reset before next operation.

4.14 Page Program Operation
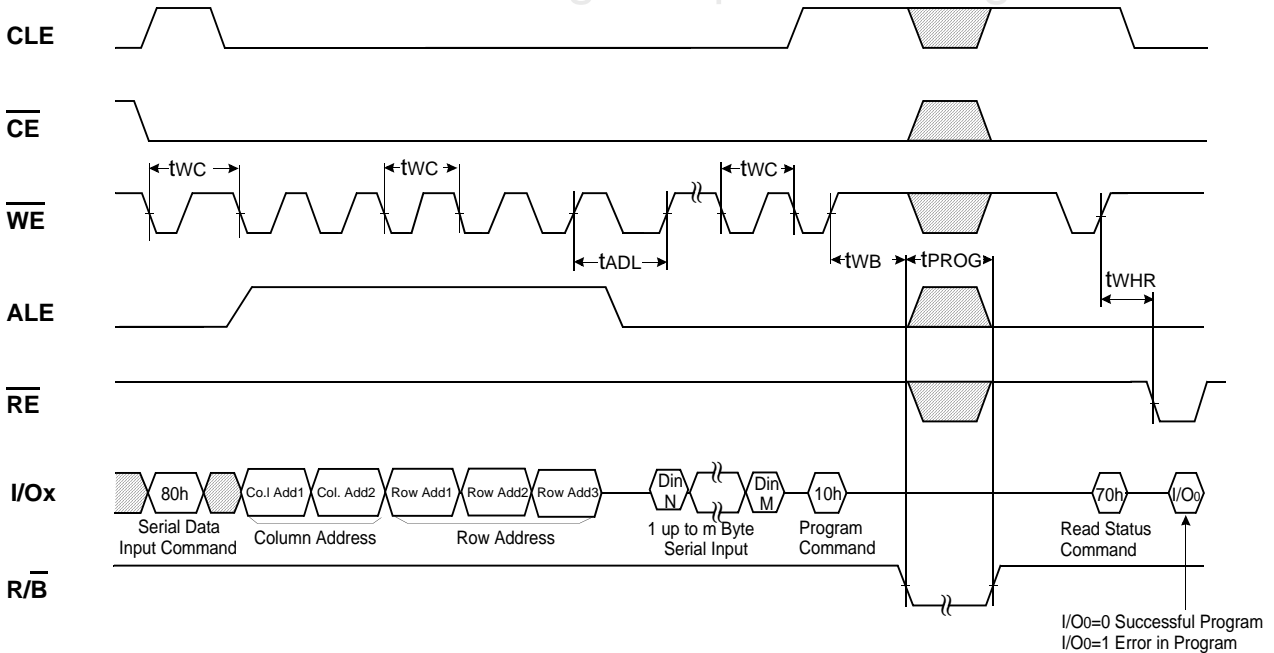
NOTE :
tADL is the time from the WE rising edge of final address cycle to the WE rising edge of first data cycle.

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4.15 Page Program Operation with Random Data Input

NOTE :
1) tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.
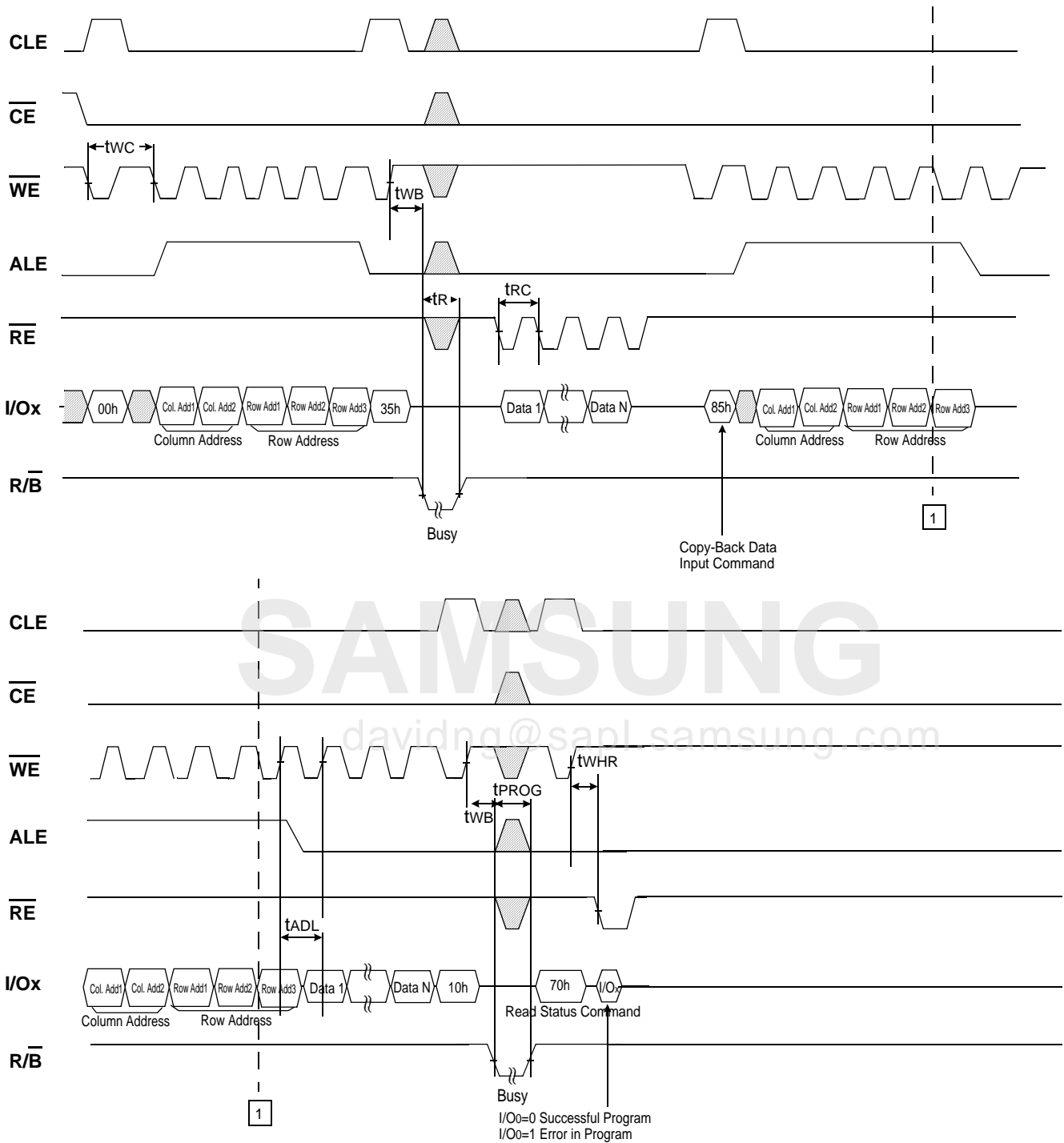
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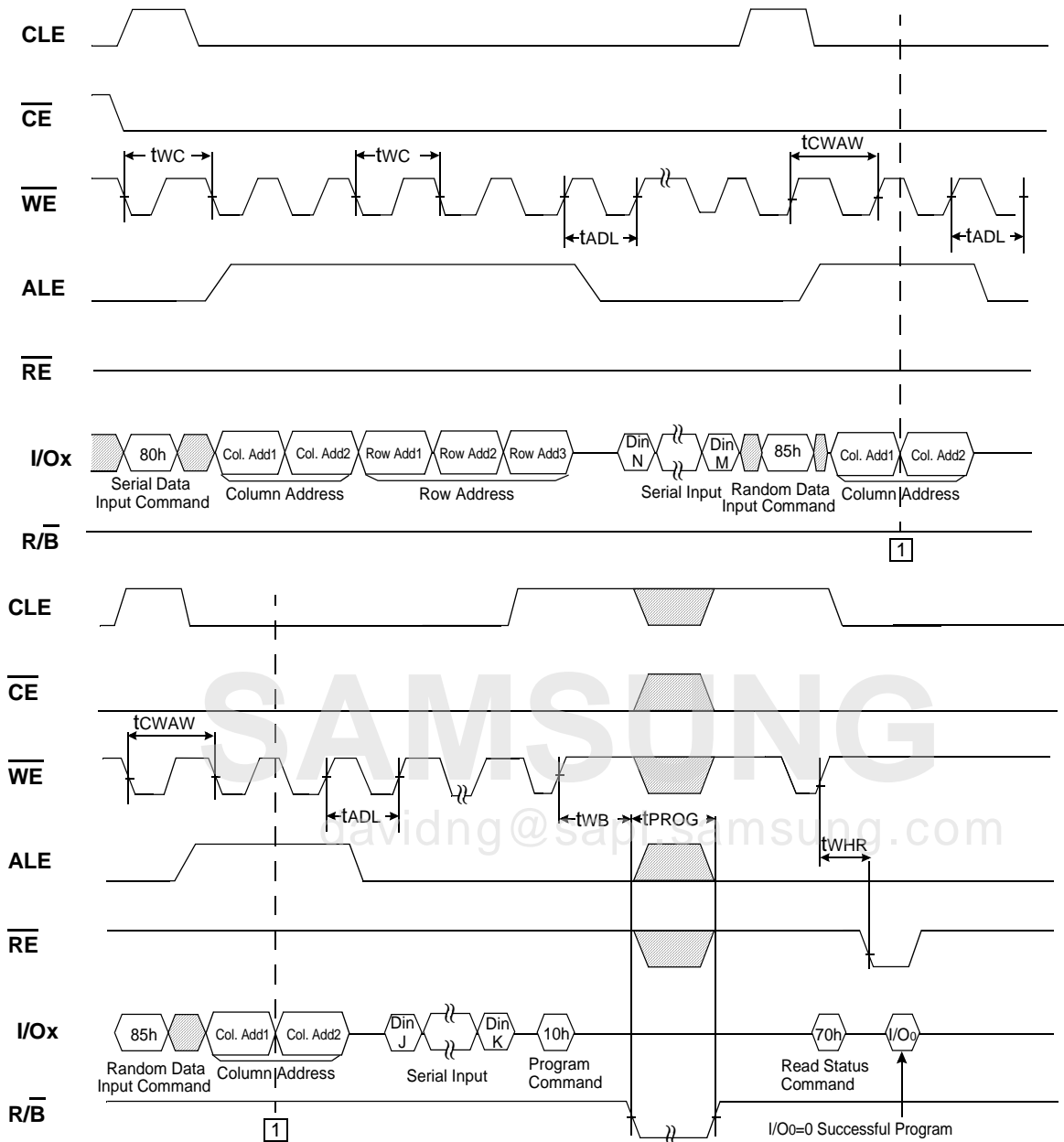
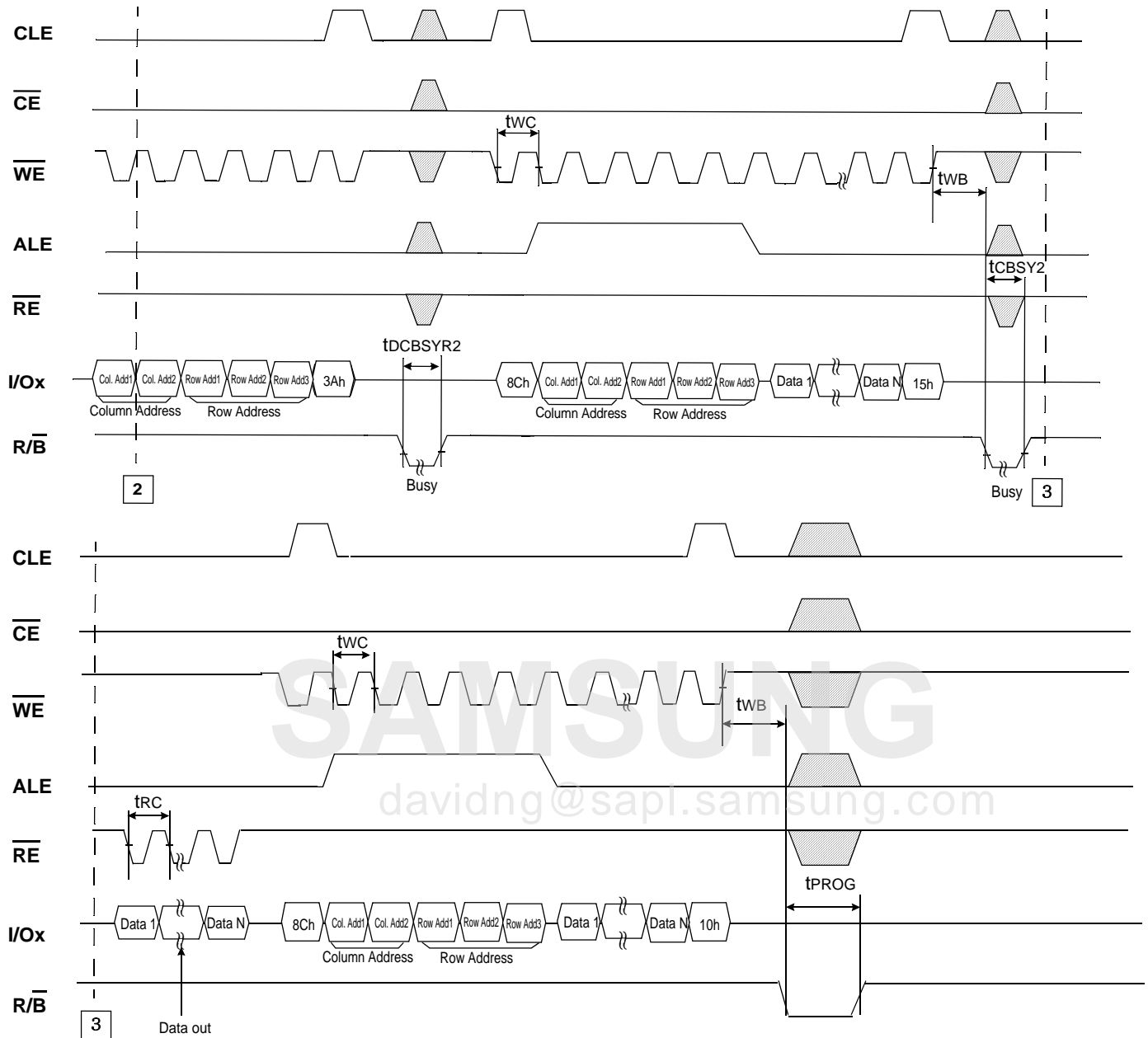## 4.16 Copy-Back Program Operation with Random Data Input

NOTE :
1) tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.
2) Copy-Back Program operation is allowed only within the same memory plane.

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4.17 Intelligent Copy-Back Program(1/2)

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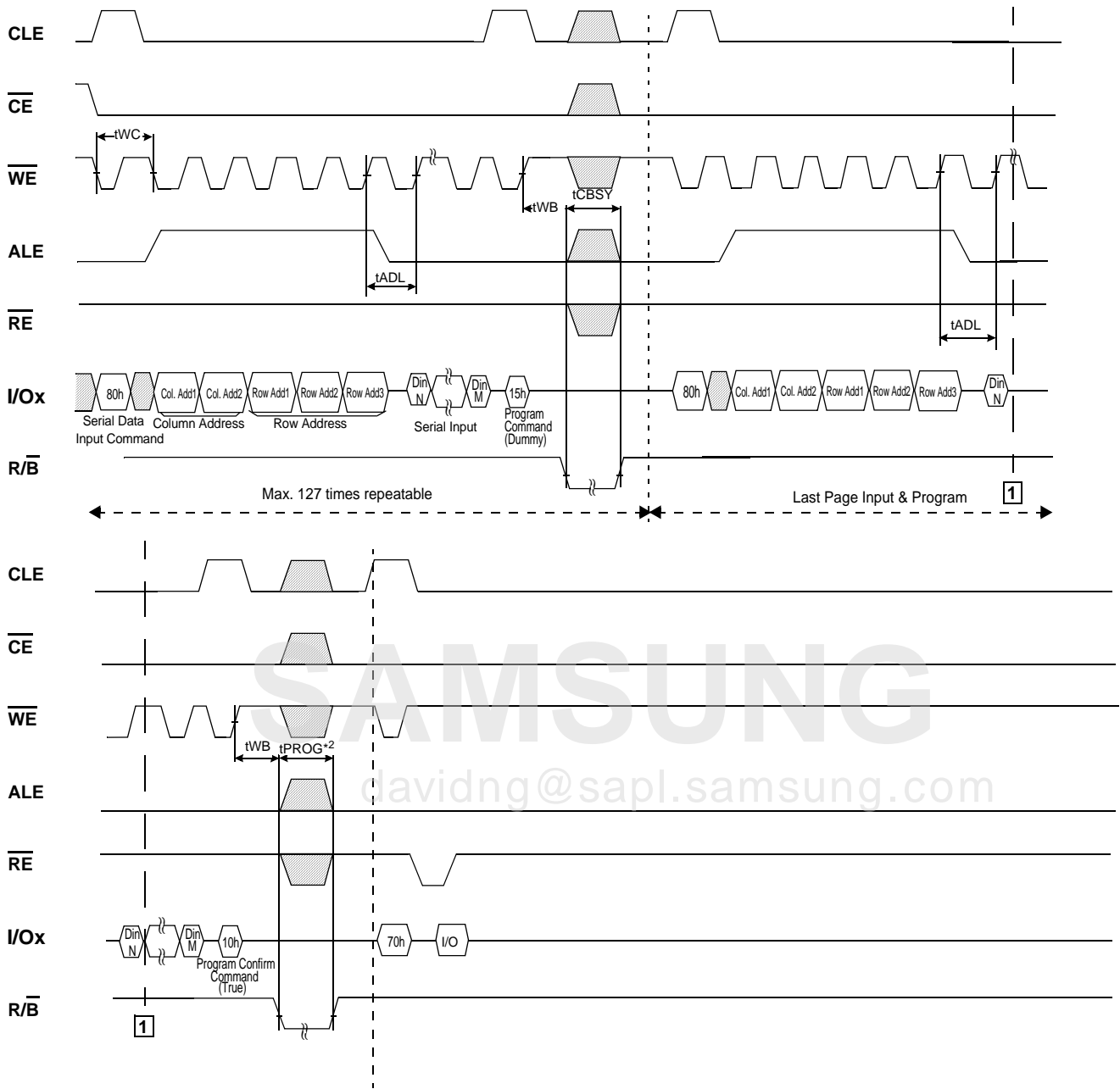
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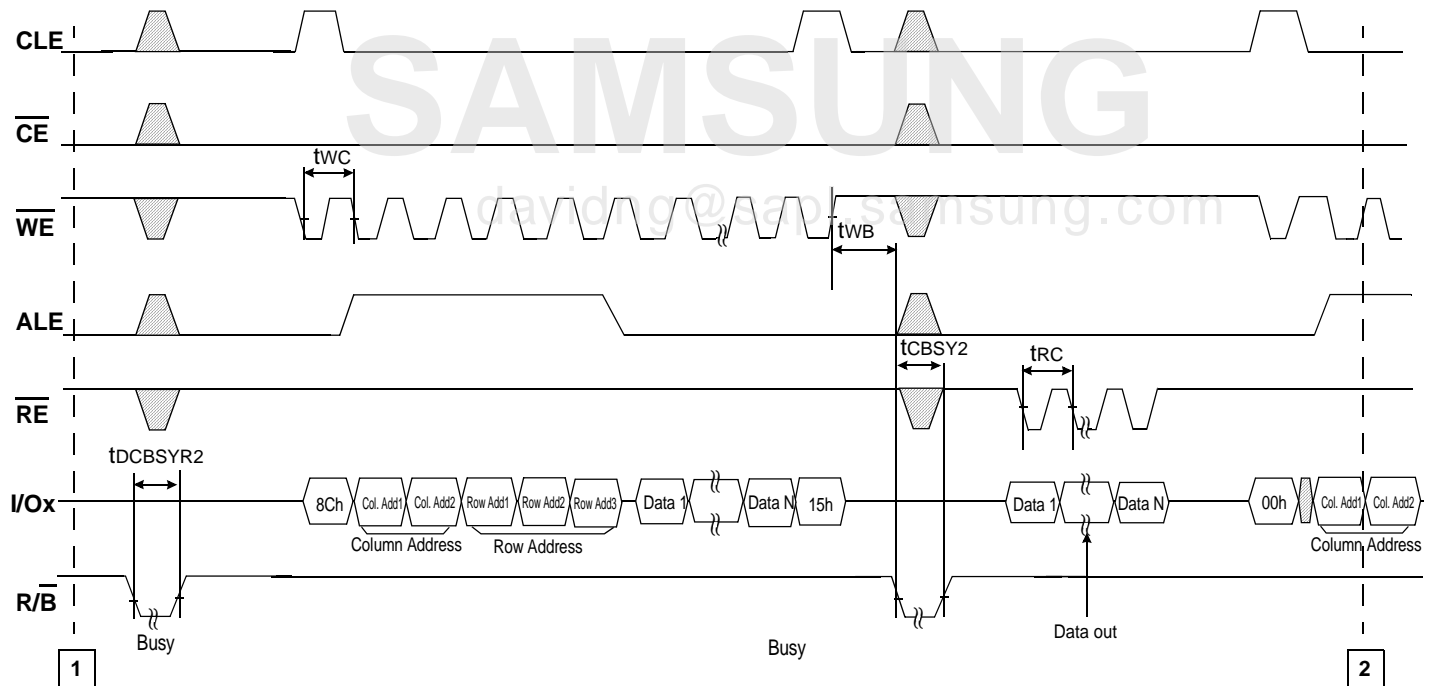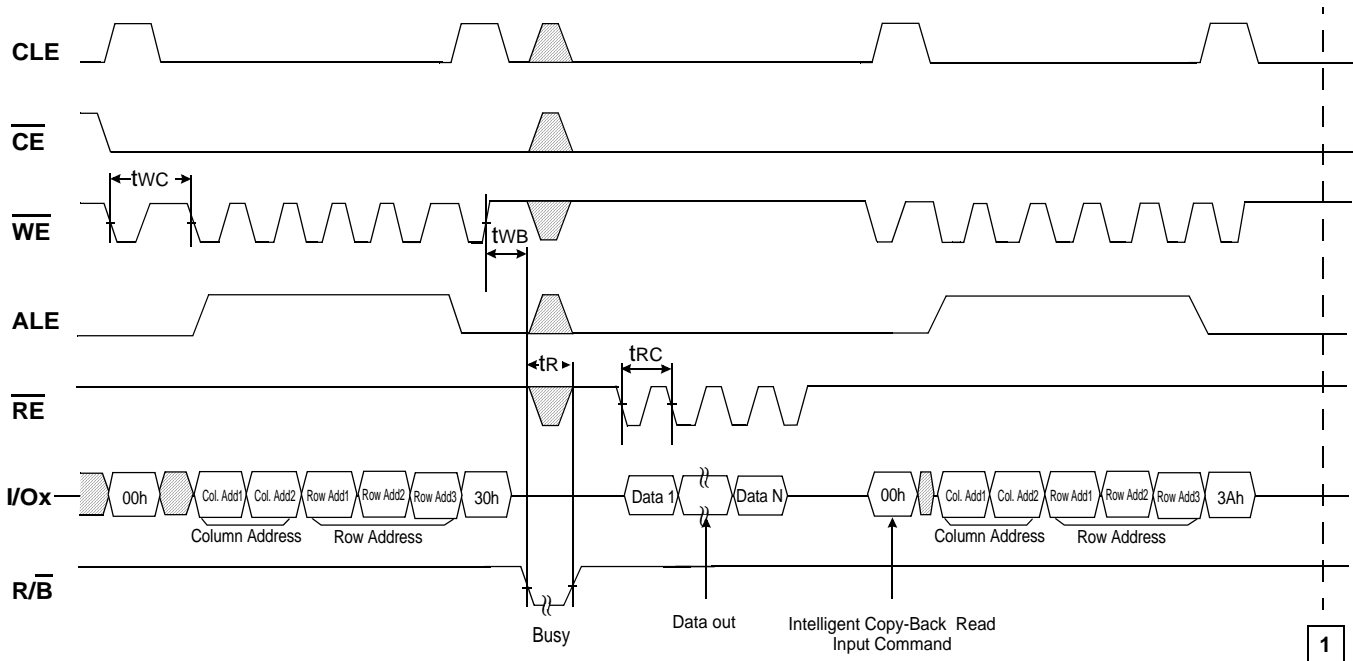
Intelligent Copy-Back Program(2/2)

NOTE :
1) Intelligent copy-Back Program operation is allowed only within the same memory plane.

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4.18 Cache Program Operation(available only within a block)

NOTE :

1) tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.

2) Since programming the last page does not employ caching, the program time has to be that of Page Program. However, if the previous program cycle with the cache data has not finished,
   the actual program cycle of the last page is initiated only after completion of the previous cycle, which can be expressed as the following formula.

   tPROG = Program time for the last page + Program time for the (last -1)[th] page - (command input cycle time + address input cycle time + Last page data loading time)
   Maximum tPROG is 10ms in this case.

e.g.) Cache Program

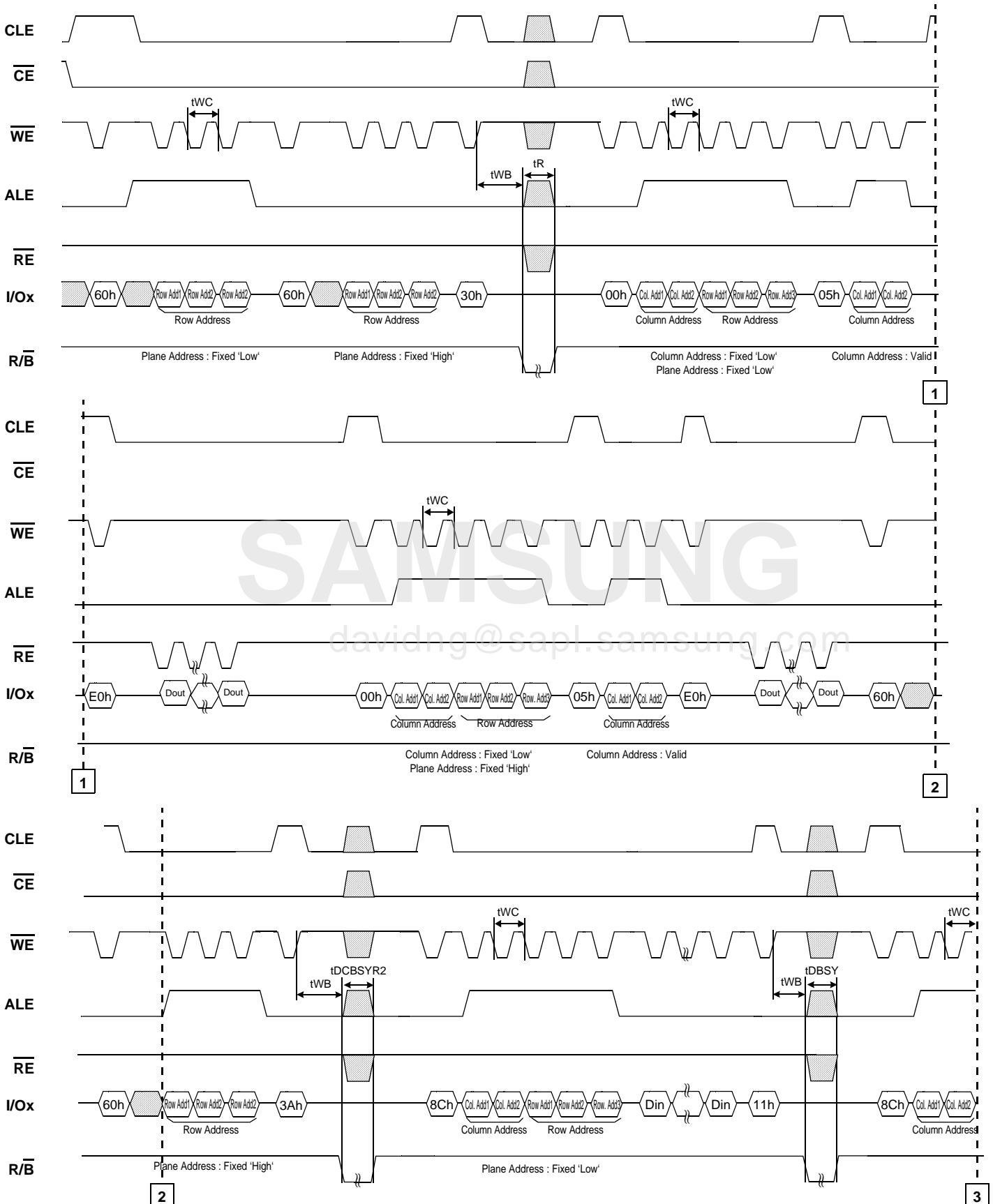SAMSUNG CONFIDENTIAL
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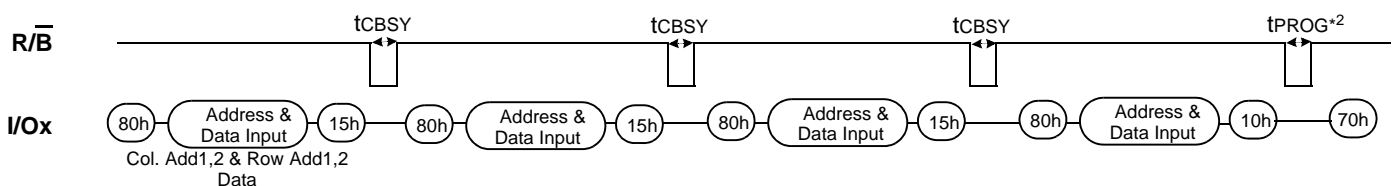
4.19 Two-Plane Copy-Back Program

NOTE :
1) Copy-Back Program operation is allowed only within the same memory plane.

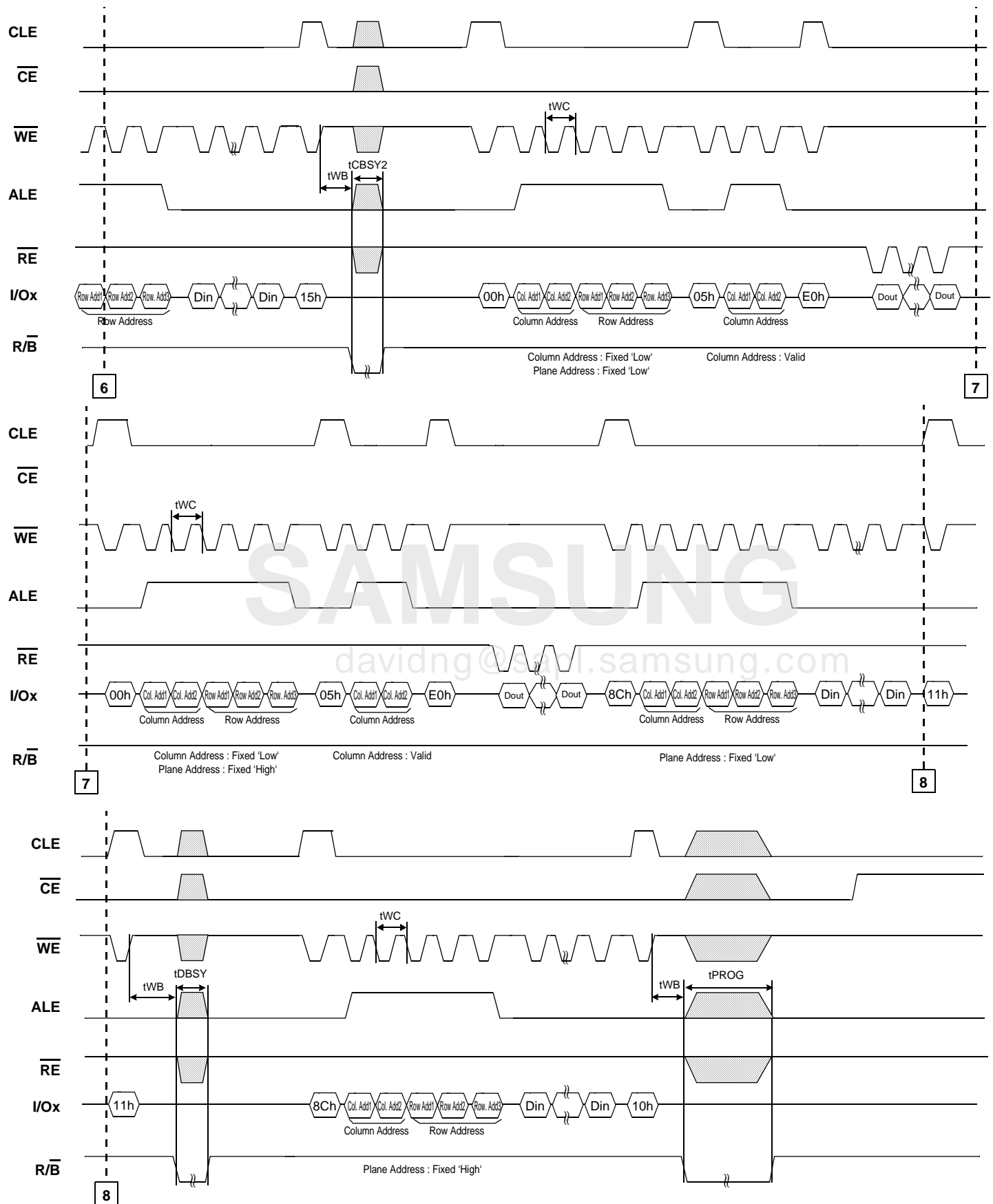SAMSUNG CONFIDENTIAL
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4.20 Two-Plane Intelligent Copy-Back Program(1/3)

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Two-Plane Intelligent Copy-Back Program(2/3)

CLE

$\overline{CE}$

$\overline{WE}$

ALE

$\overline{RE}$

I/Ox

R/$\overline{B}$

tWC

tWC

tWB   tCBSY2

Col. Add2 Row Add1 Row Add2 Row. Add3 Din Din 15h   00h Col. Add1 Col. Add2 Row Add1 Row Add2 Row. Add3 05h Col. Add1 Col. Add2 E0h

Row Address   Column Address   Row Address   Column Address

Plane Address : Fixed 'High'   Column Address : Fixed 'Low'   Column Address : Valid
Plane Address : Fixed 'Low'

3   4

CLE

$\overline{CE}$

$\overline{WE}$

ALE

$\overline{RE}$

I/Ox

R/$\overline{B}$

tWC

tWC

Dout Dout 00h Col. Add1 Col. Add2 Row Add1 Row Add2 Row. Add3 05h Col. Add1 Col. Add2 E0h Dout Dout 60h Row Add1 Row Add2 Row Add2 60h

Column Address   Row Address   Column Address   Row Address

Column Address : Fixed 'Low'   Column Address : Valid   Plane Address : Fixed 'Low'
Plane Address : Fixed 'High'

4   5

CLE

$\overline{CE}$

$\overline{WE}$

ALE

RE

I/Ox

R/$\overline{B}$

tWC

tDCBSYR2   tDBSY

tWB   tWB

Row Add1 Row Add2 Row Add2 3Ah   8Ch Col. Add1 Col. Add2 Row Add1 Row Add2 Row. Add3 Din Din 11h   8Ch Col. Add1 Col. Add2 Row Add1

Row Address   Column Address   Row Address   Column Address

Plane Address : Fixed 'High'   Plane Address : Fixed 'Low'   Plane Address : Fixed 'High'

5   6

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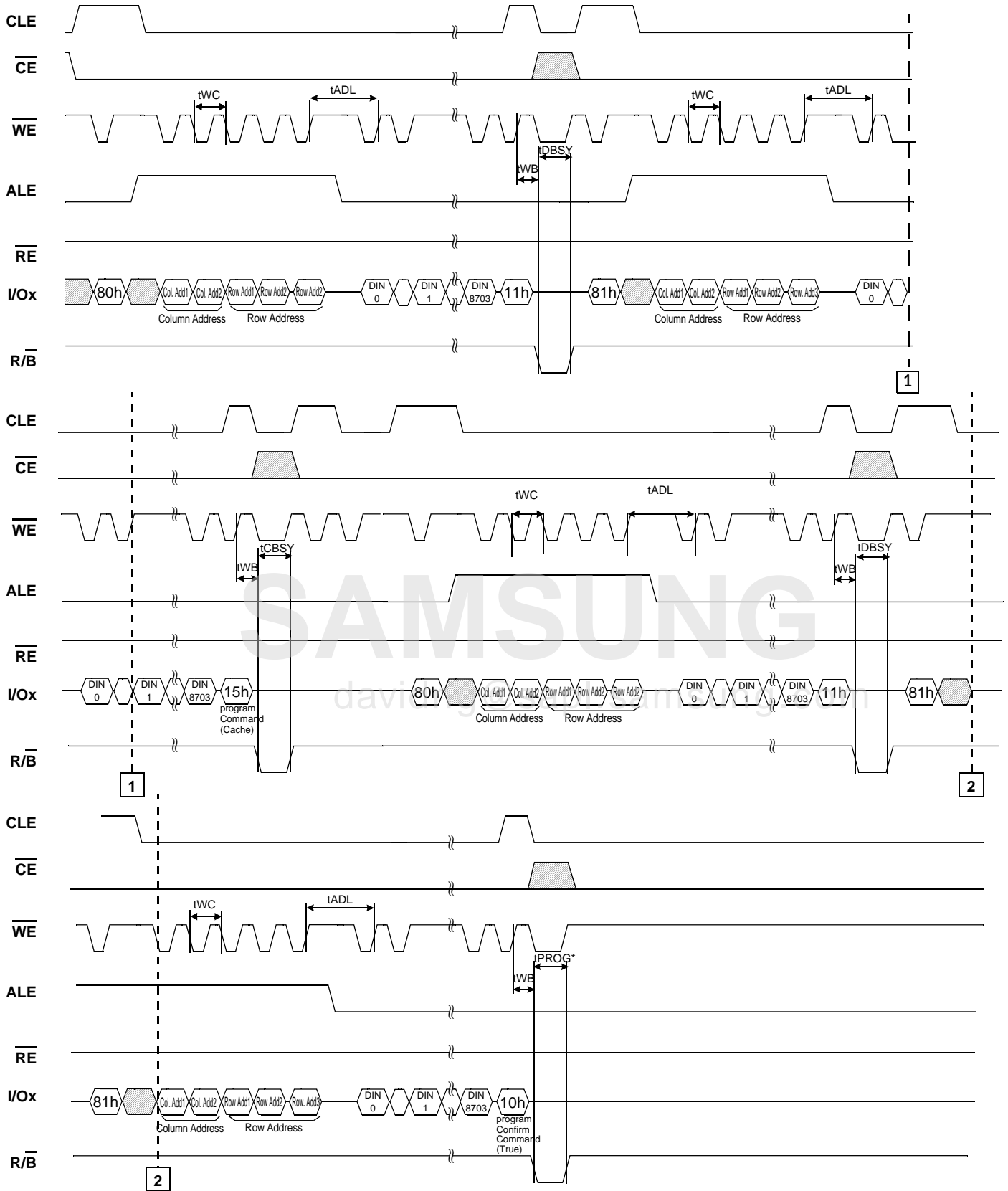## Two-Plane Intelligent Copy-Back Program(3/3)

NOTE :
1) Intelligent copy-Back Program operation is allowed only within the same memory plane.

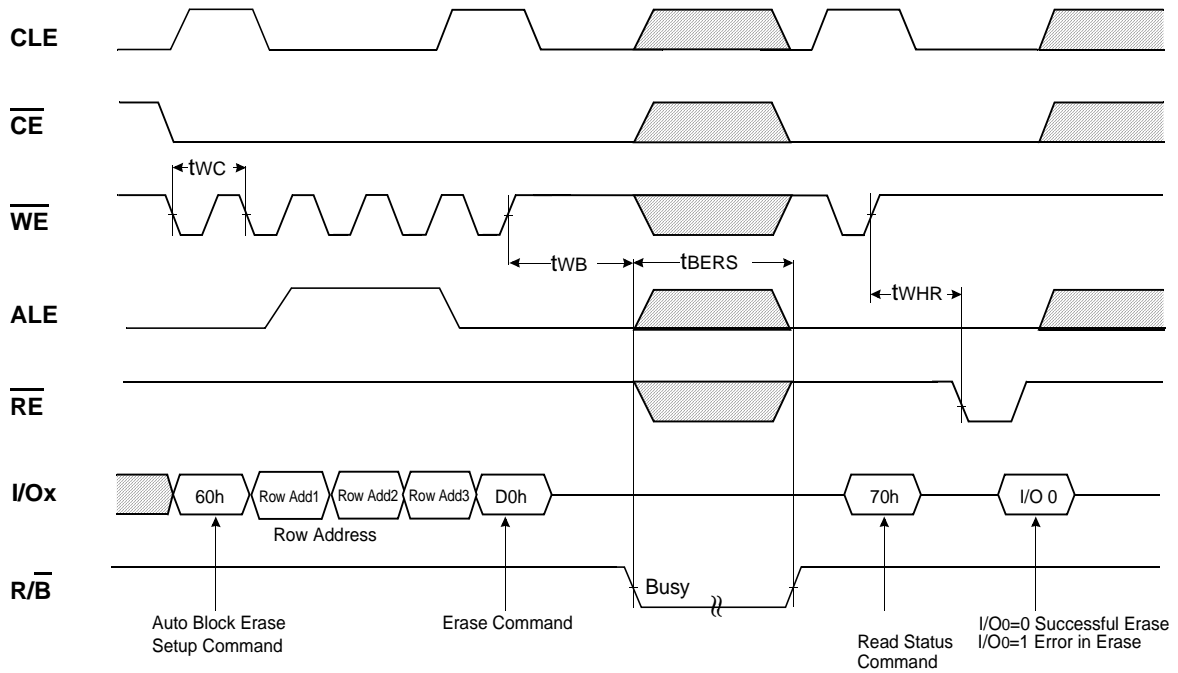**SAMSUNG CONFIDENTIAL**
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4.21 Two-Plane Page Program Operation

e.g.) Two-Plane Page Program

column address : Valid
page address : Page M
plane address : Fixed 'Low'
block address : Block N

column address : Valid
page address : Page M
plane address : Fixed 'High'
block address : Block N

NOTE :
Any command between 11h and 81h is prohibited except 70h/F1h/F2h and FFh.

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4.22 Two-Plane Cache Program Operation

NOTE :
1) tPROG = Program time for the last page + Program time for the (last -1)[th] page - (command input cycle time + address input cycle time + Last page data loading time)
2) Make sure to terminate the operation with 80h-10h- command sequence. If the operation is terminated by 80h-15h command sequence, monitor I/O 6 (Ready/Busy) by issu-ing Status Read Command (70h/F1h/F2h) and make sure the previous page program operation is completed. If the page program operation is completed issue FFh reset before next operation.
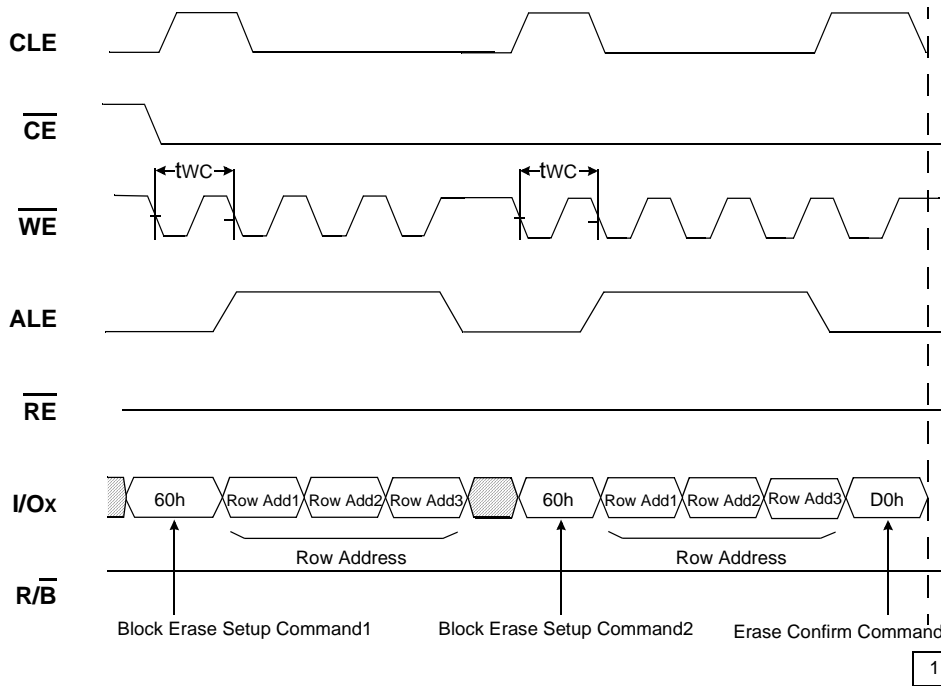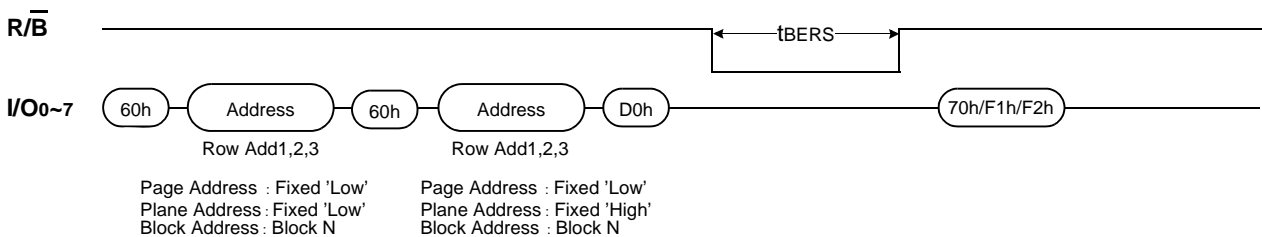
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4.23 Block Erase Operation

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4.24 Two-Plane Block Erase Operation

Block Erase Setup Command1   Block Erase Setup Command2   Erase Confirm Command

Erase Confirm Command

I/O 0 = 0 Successful Erase
I/O 0 = 1 Error in Erase

Read Status Command
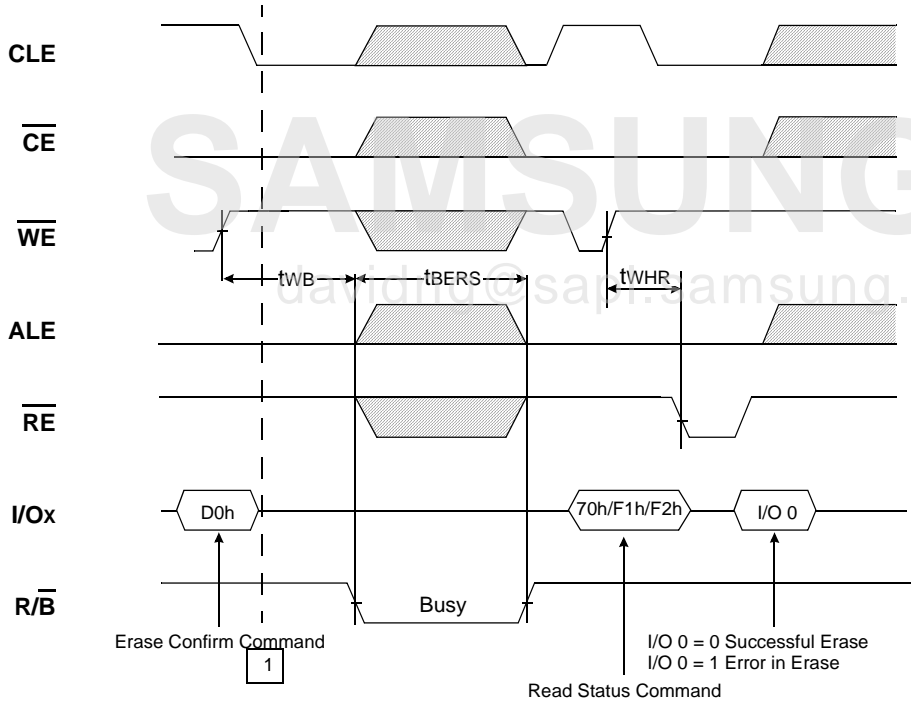
e.g.) Address Restriction for Two-Plane Block Erase Operation

Page Address : Fixed 'Low'   Page Address : Fixed 'Low'
Plane Address : Fixed 'Low'   Plane Address : Fixed 'High'
Block Address : Block N   Block Address : Block N

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4.25 Read ID Operation
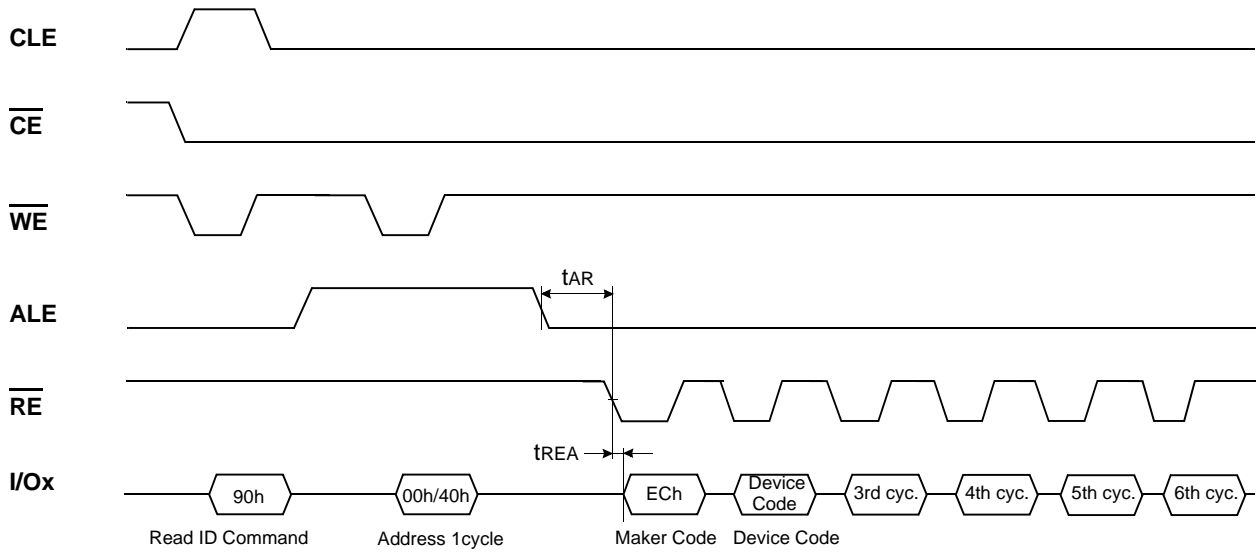
NOTE :
1) Address 00h is for Samsung legacy and 40h is for new JEDEC ID informat

4.26 00h Address ID Cycle

Device	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
K9GBG08U0B	ECh	D7h	94h	7Eh	64h	44h
K9LCG08U0B	ECh	DEh	D5h		68h	

4.27 40h Address ID Cycle

Device	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
K9XXG08U0B	4Ah	45h	44h	45h	43h	01h

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00h Address ID Definition Table

	Description
1st Byte	Maker Code
2nd Byte	Device Code
3rd Byte	Internal Chip Number, Cell Type, Number of Simultaneously Programmed Pages, Etc.
4th Byte	Page Size, Block Size,Redundant Area Size.
5th Byte	Plane Number, ECC Level, Organization.
6th Byte	Device Technology, EDO, Interface.

3rd ID Data

Description		IO7	IO6	IO5 IO4	IO3 IO2	IO1 IO0
Internal Chip Number	1 2 4 8					0 0 0 1 1 0 1 1
Cell Type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell				0 0 0 1 1 0 1 1	
Number of Simultaneously Programmed Pages	1 2 4 8			0 0 0 1 1 0 1 1		
Interleaving operation between multiple chips	Not Support Support		0 1			
Cache Program	Not Support Support	0 1				

4th ID Data

Description		IO7	IO6	IO5 IO4	IO3	IO2	IO1 IO0
Page Size (w/o redundant area)	2KB 4KB 8KB Reserved						0 0 0 1 1 0 1 1
Block Size (w/o redundant area)	128KB 256KB 512KB 1MB Reserved Reserved Reserved Reserved	0 0 0 0 1 1 1 1		0 0 0 1 1 0 1 1 0 0 0 1 1 0 1 1			
Redundant Area Size (byte / Page Size)	Reserved 128B 218B 400B 436B 512B 640B Reserved		0 0 0 0 1 1 1 1		0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1	

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5th ID Data

Description		I/O7	I/O6	I/O5	I/O4	I/O3	I/O2		I/O1
Plane Number	1 2 4 8 16		-			0 0 1 1 1	0 1 0 1 1	0 0 0 0 1	
ECC Level	1bit 2bit 4bit 8bit 16bit 24bit 40bit 60bit		0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1				
Reserved		0							0

6th ID Data

Description		I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Device Version	50nm 40nm 30nm 2xnm 2ynm Reserved Reserved Reserved						0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 0
EDO	Not Support Support		0 1						
Interface	Conventional Mode Toggle Mode	0 1							
Reserved				0	0	0			

40h Address ID Definition Table

Byte	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
0	J	0	1	0	0	1	0	1	0
1	E	0	1	0	0	0	1	0	1
2	D	0	1	0	0	0	1	0	0
3	E	0	1	0	0	0	1	0	1
4	C	0	1	0	0	0	0	1	1
5	Legacy Asynchronous SDR Toggle Mode DDR Synchronous DDR	0	0	0	0	0 0 0	0 0 1	0 1 0	1 0 0

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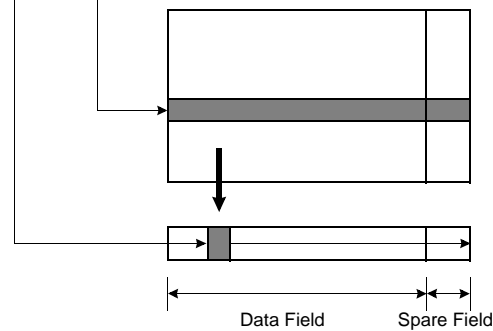
5.0 DEVICE OPERATION

5.1 Page Read

Page read is initiated by writing 00h-30h to the command register along with five address cycles. The 8,704 bytes of data within the selected page are transferred to the cache registers via data registers in less than tR. The system controller can detect the completion of this data transfer(tR) by analyzing the output of R/B̄ pin. Once the data in a page is loaded into the cache registers, they may be read out in Read cycle time(tRC) by sequentially pulsing RE. The repetitive high to low transitions of the RE clock make the device output the data starting from the selected column address up to the last column address.

The device may output random data in a page instead of the consecutive sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page.

Read Operation

Col. Add.1,2 & Row Add.1,2,3

Data Field   Spare Field

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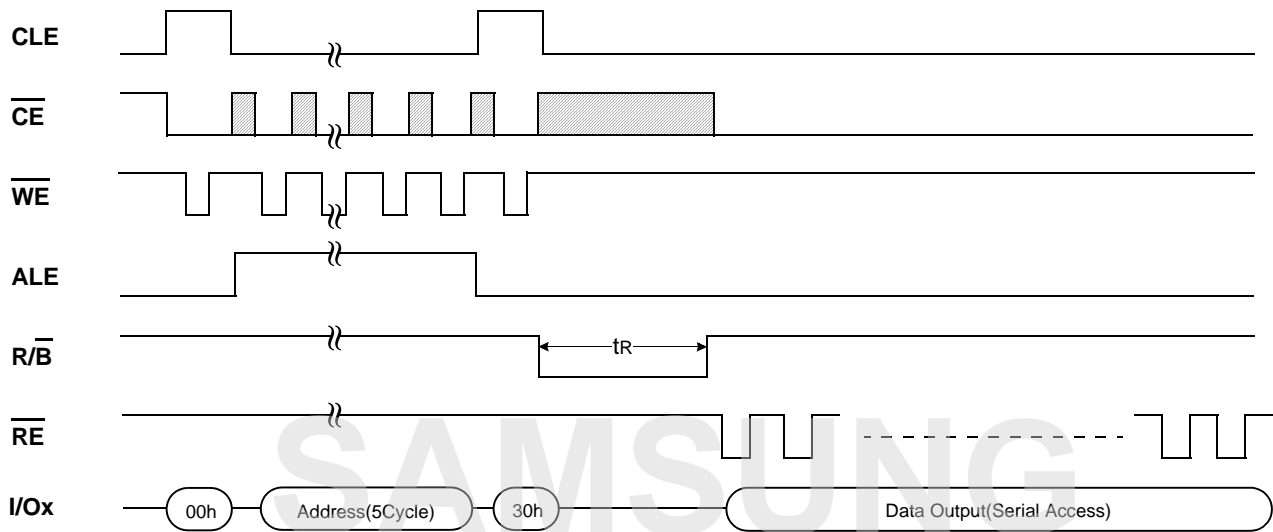
Random Data Output In a Page
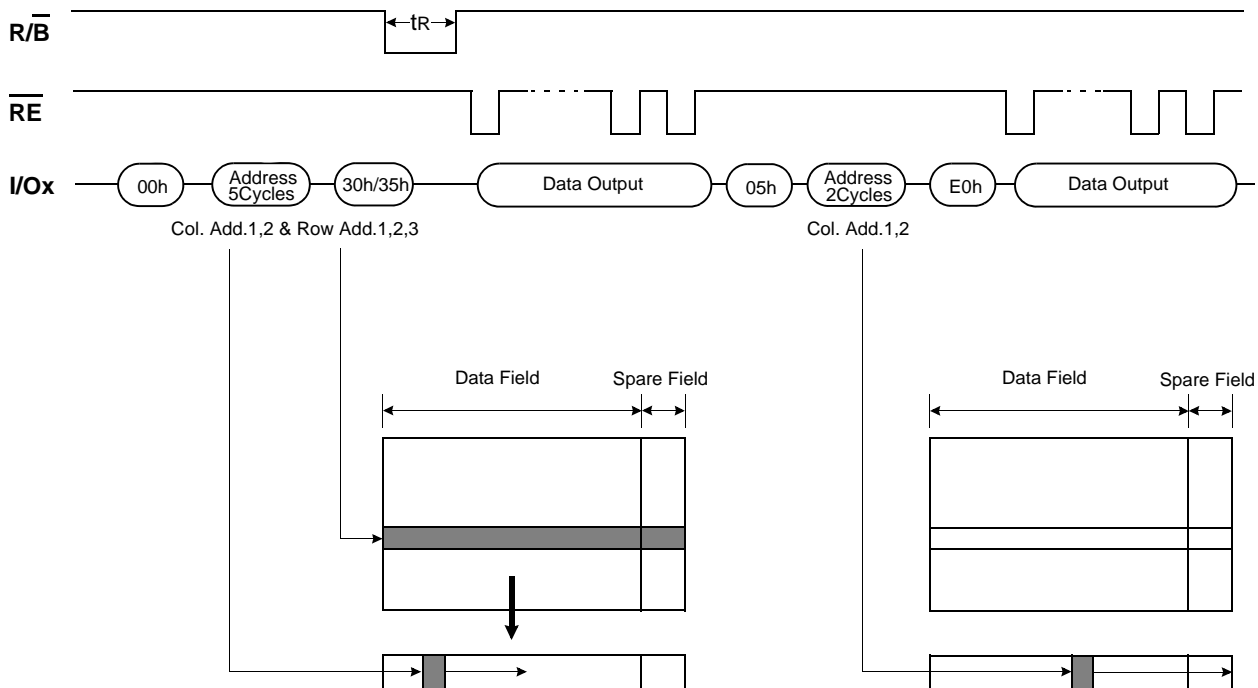
5.2 Cache Read

Cache Read is an extension of Page Read, which is executed with 8,704byte data registers, and is available only within a block. Since the device has 1 page of cache memory, serial data output may be executed while data in the memory cell is read into data registers.

Cache read is also initiated by writing 00h-30h to the command register along with five address cycles. After initial power up, 00h command is latched. Therefore only five address cycles and 30h command initiates that operation after initial power up. The 8,704 bytes of data within the selected page are transferred to the cache registers via data registers in less than tR. After issuing Cache Read command(31h), read data in the data registers is transferred to cache registers for a short period of time(t_{DCBSYR}). While the data in the cache registers is read out in Read cycle time(tRC) by sequentially pulsing $\overline{RE}$, data of next page is transferred to the data registers. By issuing Last Cache Read command(3Fh), last data is transferred to the cache registers from the data registers after the completion of transfer from memory cell to data registers.

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Cache Read

The device has a Read operation with cache registers that enables the high speed read operation shown below. When the block address changes, this sequence has to be started from the beginning.
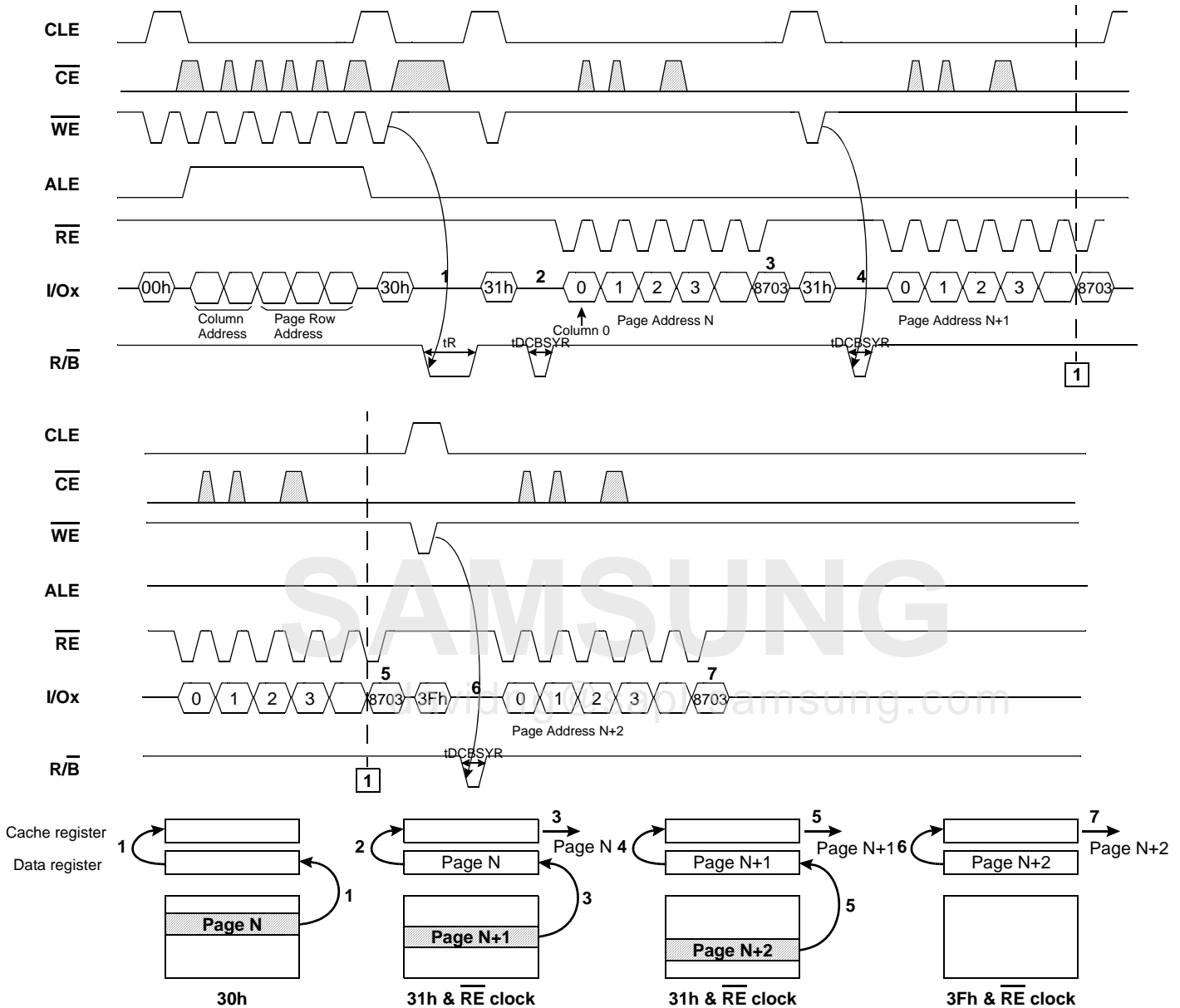
NOTE :
-. If the 31h command is issued to the device, the data content of the next page is transferred to the data registers during serial data out from the cache registers, and therefore the tR (Data transfer from memory cell to data register) will be reduced.

1) Normal read. Data is transferred from Page N to cache registers through data registers. During this time period, the device outputs Busy state for tR max.
2) After the Ready/Busy returns to Ready, 31h command is issued and data is transferred to cache registers from data registers again. This data transfer takes tDCBSYR max and the completion of this time period can be detected by Ready/Busy signal.
3) Data of Page N+1 is transferred to data registers from cell while the data of Page N in cache registers can be read out by $\overline{RE}$ clock simultaneously.
4) The 31h command makes data of Page N+1 transfer to cache registers from data registers after the completion of the transfer from cell to data registers. The device outputs Busy state for tDCBSYR max..This Busy period depends on the combination of the internal data transfer time from cell to data registers and the serial data out time.
5) Data of Page N+2 is transferred to data registers from cell while the data of Page N+1 in cache registers can be read out by $\overline{RE}$ clock simultaneously.
6) The 3Fh command makes the data of Page N+2 transfer to the cache registers from the data registers after the completion of transfer from cell to data registers. The device outputs Busy state for tDCBSYR max.This Busy period depends on the combination of the internal data transfer time from cell to data registers and the transfer from data registers to cache registers.
7) Data of Page N+2 in cache registers can be read out, but since the 3Fh command does not transfer the data from the memory cell to data registers, the device can accept new command input immediately after the completion of serial data out.

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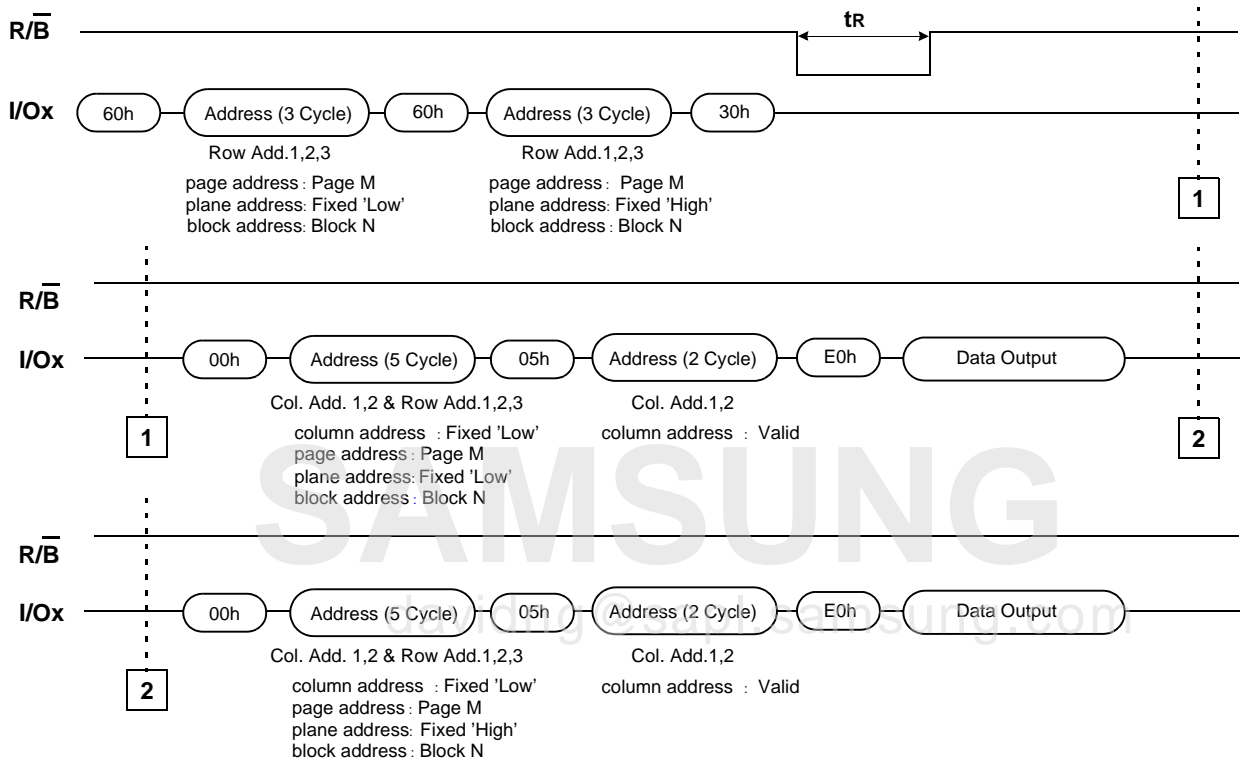**FLASH MEMORY**

5.3 Two-plane Page Read

Two-Plane Page Read is an extension of Page Read, for a single plane with 8,704 byte data registers. Since the device is two memory plane based, activating the two sets of 8,704 byte data registers enables two pages in a row at the same time. Two-Plane Page Read is initiated by writing 60h command with three address cycles twice. In this case, only same page of same block can be selected from each plane.

After Read Confirm command(30h), the 17,408bytes of data within the selected two page are transferred to the data registers in less than tR. The system controller can detect the completion of data transfer(tR) by monitoring the output of R/B pin.

Once the data is loaded into the data registers, the data output of first plane can be read out with a following sequence: command 00h - five address cycles - command 05h - two column address - command E0h. The data output of second plane can be read out using the identical command/address sequence.

Two-Plane Read must be used in the block which is programmed with Two-Plane Page Program.

Two-Plane Page Read Operation with Two-Plane Random Data Out

**Unaligned Two- Plane Page Read Operation**
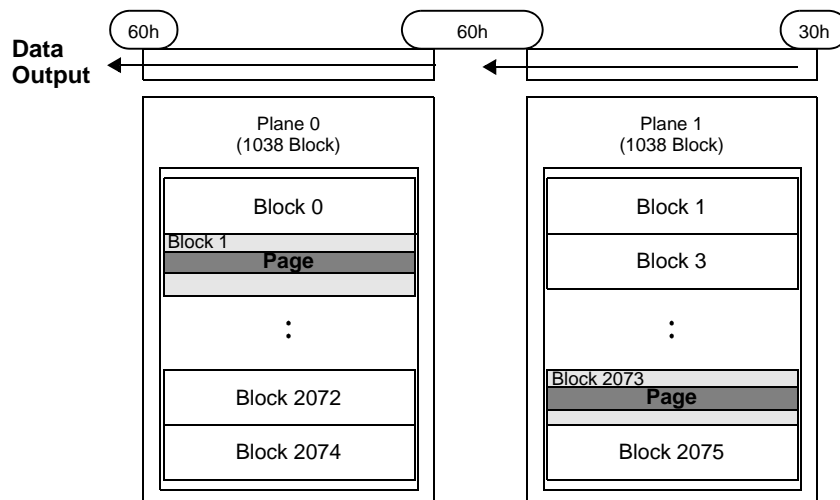
NOTE :
1) Two-Plane page Read operation shall be supported in unaligned block address, as long as address are same in all pages.

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5.4 Two-plane Cache Read

Two-Plane Cache Read is an extension of Cache Read, for a single plane with 8,704 byte data registers. Since the device is two memory plane based, activating the two sets of 8,704 byte data registers enables a cache read of two pages. Two-Plane Cache Read is initiated by repeating command 60h followed by three address cycles twice. In this case only same page of same block can be selected from each plane.

After Read Confirm command(33h) the 17,408 bytes of data within the selected two page are transferred to the cache registers via data registers in less than tR. After issuing Cache Read command(31h), read data in the data registers is transferred to cache registers for a short period of time(tDCBSYR). Once the data is loaded into the cache registers from data registers, the data output of first plane can be read out by issuing command 00h with Five Address Cycles, command 05h with two column address and finally E0h. The data output of second plane can be read out using the identical command sequences. The detail sequence of Two-Plane Cache Read is shown below.

Two-Plane Cache Read Operation with Two-Plane Random Data Out

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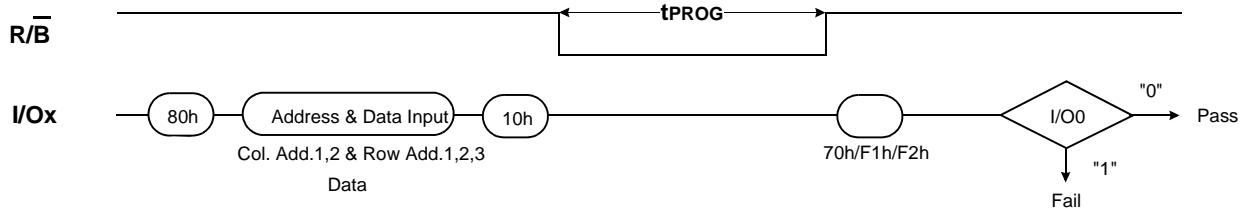
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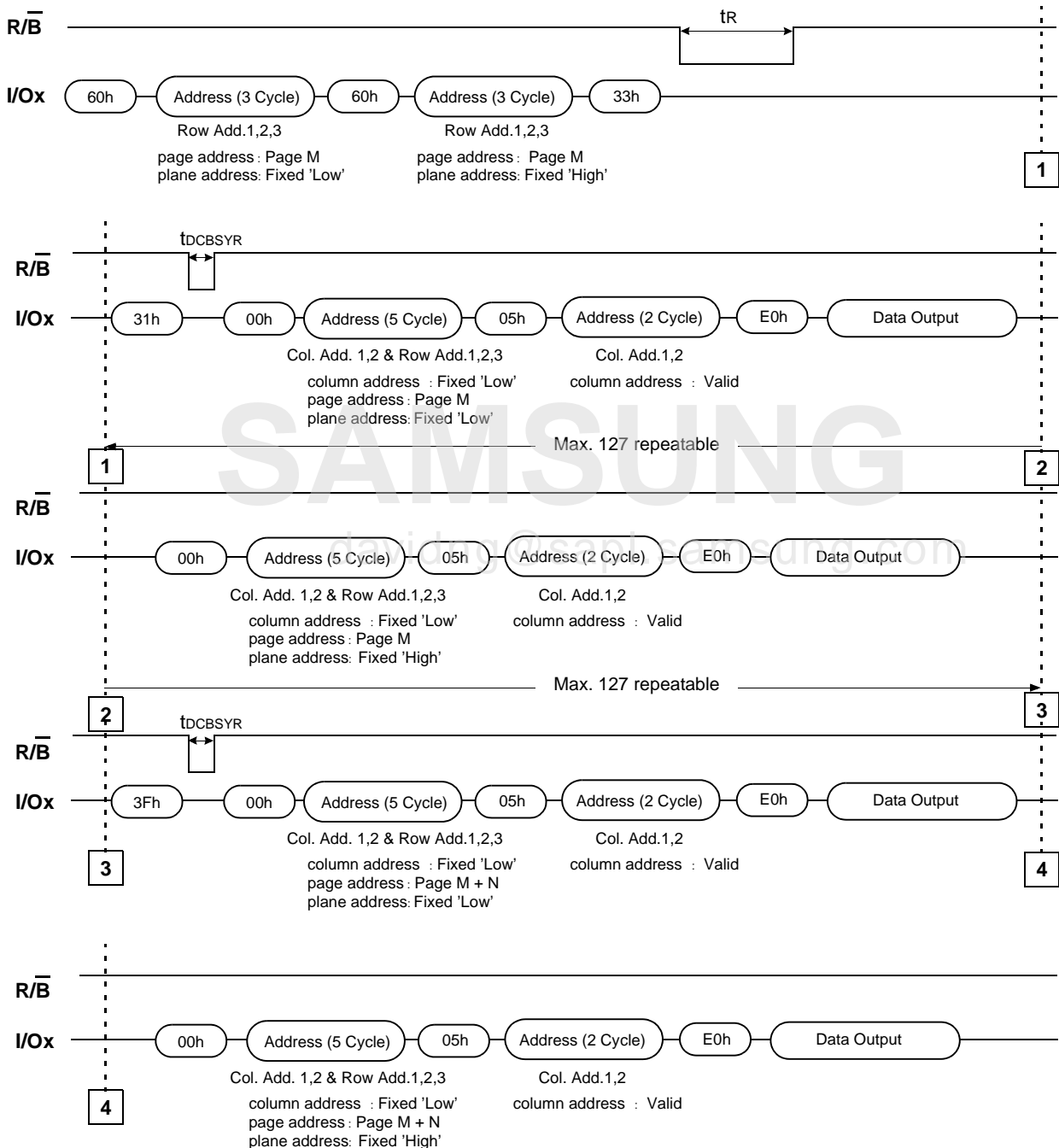
5.5 Page Program

The device is programmed basically on a page basis, and the number of consecutive partial page programming operation within the same page without an intervening erase operation(NOP) must not exceed 1 time for the page, and partial programming less than the minimum randomization unit is not allowed. Also, unwritten sectors in a page must be loaded with randomized data before program operation. The addressing should be done in sequential order in a block. A page program cycle consists of a serial data loading period in which up to 8,704bytes of data may be loaded into the data registers via cache registers, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell.

The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the five cycle address inputs and then serial data loading. The words other than those to be programmed do not need to be loaded. The device supports random data input in a page. The column address for the next data, which will be entered, may be changed to the address which follows random data input command(85h). Random data input may be operated multiple times regardless of how many times it is done in a page.

The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B̄ output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit(I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

Program & Read Status Operation

Random Data Input In a Page

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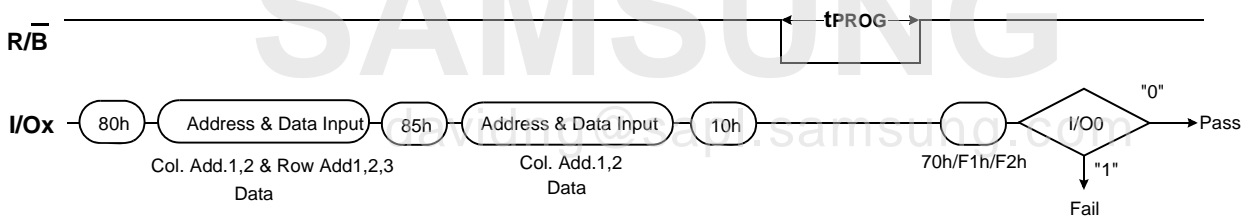
5.6 Copy-back Program

Copy-Back program with Read for Copy-Back is configured to quickly and efficiently rewrite data stored in one page without data re-loading when the bit error is not in data stored. Since the time-consuming re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also needs to be copied to the newly assigned free block. Copy-Back operation is a sequential execution of Read for Copy-Back and of copy-back program with the destination page address. A read operation with "35h" command and the address of the source page moves the whole 8,704byte data into the internal data buffer. A bit error is checked by sequential reading the data output. In the case where there is no bit error, the data do not need to be reloaded. Therefore Copy-Back program operation is initiated by issuing Page-Copy Data-Input command (85h) with destination page address. Actual programming operation begins after Program Confirm command (10h) is issued. Once the program process starts, the Read Status Register command (70h) may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B output, or the Status bit(I/O 6) of the Status Register. When the Copy-Back Program is complete, the Write Status Bit(I/O 0) may be checked. The command register remains in Read Status command mode until another valid command is written to the command register.
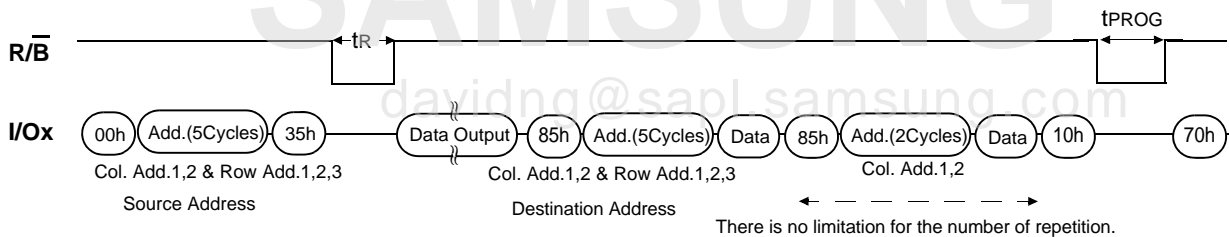
During copy-back program, data modification is possible using random data input command (85h) as shown below.
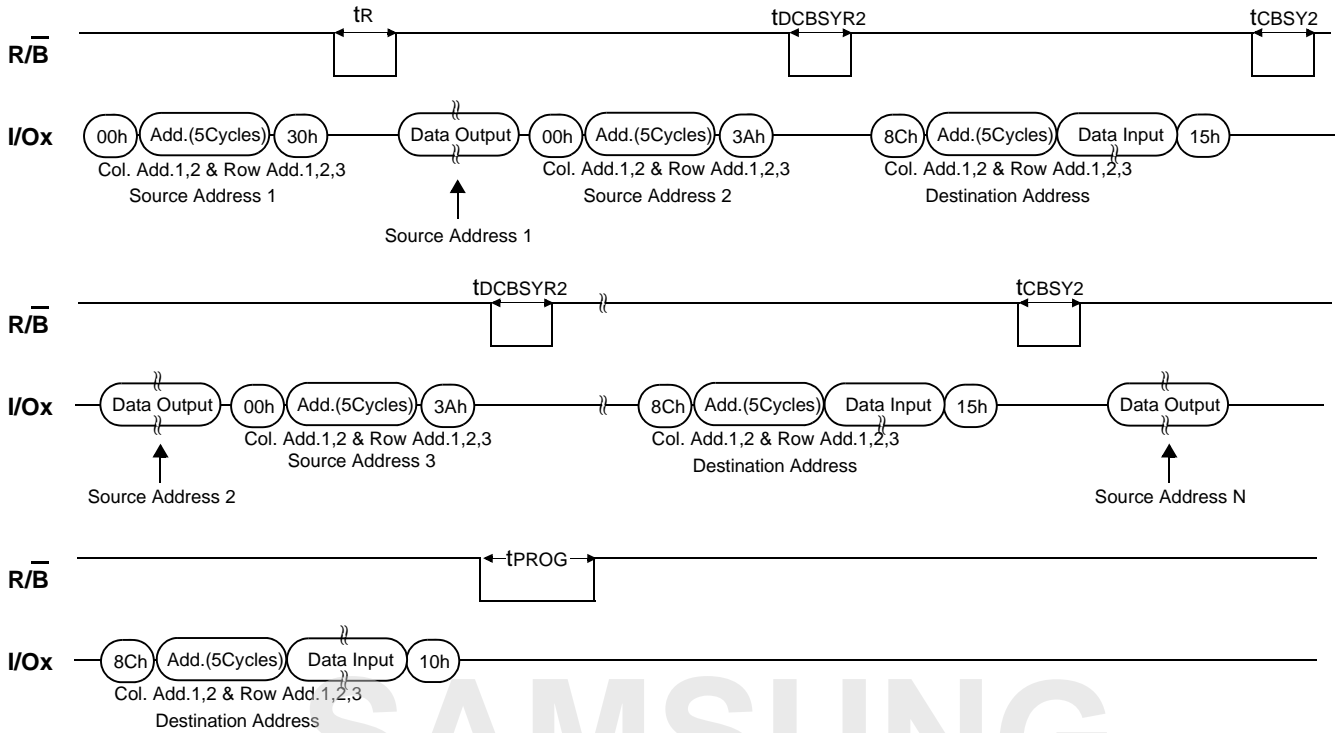
Page Copy-Back Program Operation
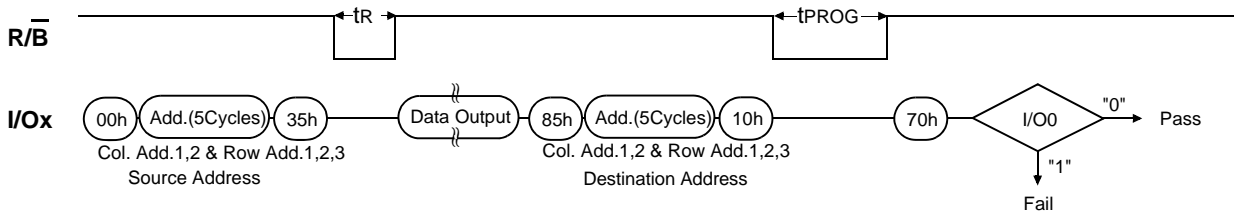
NOTE :
1) Copy-Back Program operation is allowed only within the same memory plane.

Page Copy-Back Program Operation with Random Data Input

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5.7 Intelligent Copy-Back Program

Intelligent Page Copy-Back Program Operation

NOTE :
1) Intelligent Copy-Back Program operation is allowed only within the same memory plane.

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5.8 Cache Program

Cache Program is an extension of Page Program, which is executed with 8,704byte data registers, and is available only within a block. Since the device has 1 page of cache memory, serial data input may be executed while data stored in data registers are programmed into memory cell.

After writing the first set of data up to 8,704byte into the selected cache registers, Cache Program command (15h) instead of actual Page Program (10h) is inputted to make cache registers free and to start internal program operation. To transfer data from cache registers to data registers, the device remains in Busy state for a short period of time(tCBSY) and has its cache registers ready for the next data-input while the internal programming gets started with the data loaded into data registers. Read Status command (70h/F1h/F2h) may be issued to find out when cache registers become ready by polling the Cache-Busy status bit(I/O 6). Pass/fail status of only the previous page is available upon the return to Ready state. When the next set of data is inputted with the Cache Program command, tCBSY is affected by the progress of pending internal programming. The programming of the cache registers is initiated only when the pending program cycle is finished and the data registers are available for the transfer of data from cache registers. The status bit(I/O5) for internal Ready/Busy may be polled to identify the completion of internal programming. If the system monitors the progress of programming only with R/B, the last page of the target programming sequence must be programmed with actual Page Program command (10h).
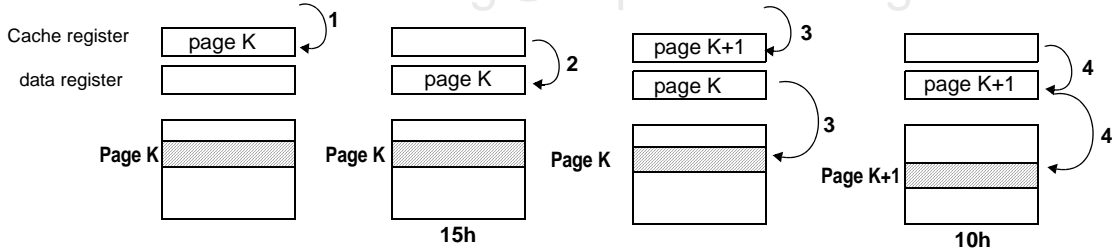
Cache Program(1/2)

NOTE :
1) Cache Program operation is available only within a block.
2) Since programming the last page does not employ caching, the program time has to be that of Page Program. However, if the previous program cycle with the cache data has not finished, the actual program cycle of the last page is initiated only after completion of the previous cycle, which can be expressed as the following formula.

tPROG = Program time for the last page + Program time for the (last -1)th page - (Program command cycle time + Last page data loading time)
Maximum tPROG is 10ms in this case.

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Cache Program(2/2)

NOTE :
- Issuing the 15h command to the device after serial data input initiates the program operation with cache registers.
1) Data for Page K is input to cache registers.
2) Data is transferred to the data registers by the 15h command. During the transfer the Ready/Busy outputs Busy State (tCBSY).
3) Data for Page K+1 is input to cache registers while the data of the Page K is being programmed.
4) The programming with cache registers is terminated by the 10h command . When the device becomes Ready, it shows that the internal programming of the Page K+1 is completed.

tPROG* = Program time for the last page + Program time for the (last -1)[th] page - (command input cycle time + address input cycle time + Last page data loading time) Maximum tPROG is 10ms in this case.

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Pass/Fail status for each page programmed by the Cache Program operation can be detected by the Read Status operation.
- I/O 0 : Pass/Fail of the current page program operation.
- I/O 1 : Pass/Fail of the previous page program operation.

The Pass/Fail status on I/O 0 and I/O 1 are valid under the following conditions.
- Status on I/O 0 : True Ready/Busy is Ready state.
    The True Ready/Busy is output on I/O 5 by Read Status operation or R/$\overline{\text{B}}$ pin after the 10h command.
- Status on I/O 1 :Cache Read/Busy is Ready State.
    The Cache Ready/Busy is output on I/O 6 by Read Status operation or R/$\overline{\text{B}}$ pin after the 15h command.
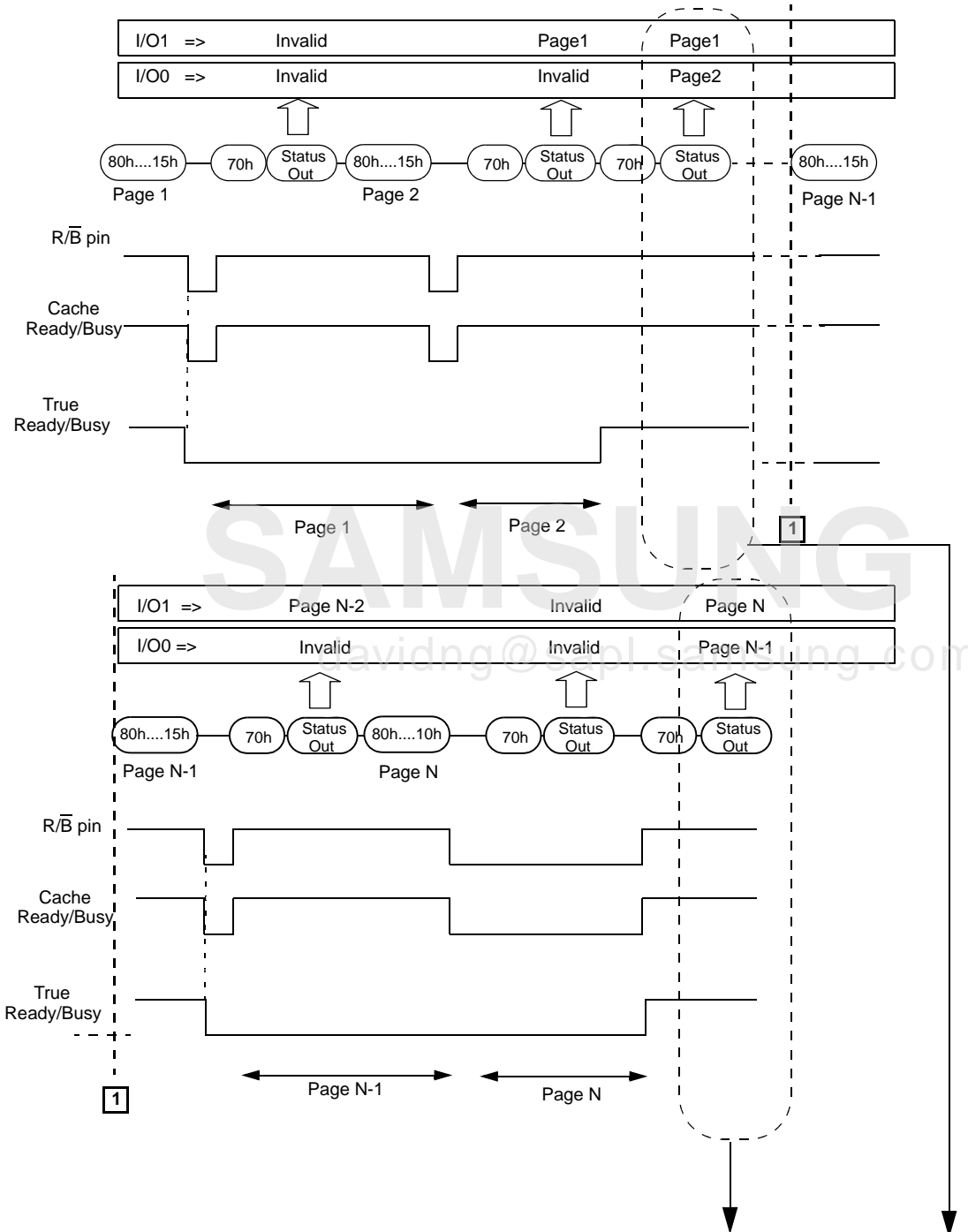
During both True Ready/Busy and Cache Ready/Busy return to Ready state, the Pass/Fail for previous page and current page can be shown through I/O 1 and I/O 0 concurrently.

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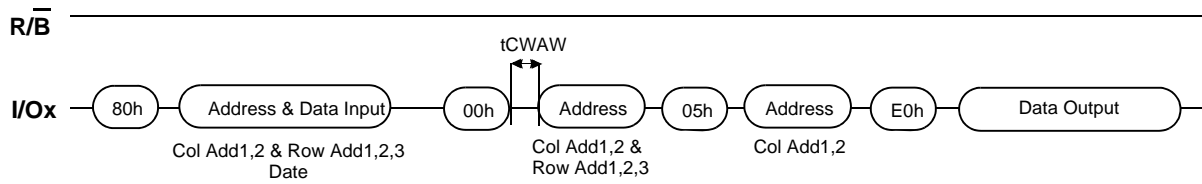datasheet

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5.9 Register Read Out Mode 1

At program operation, loaded data to the register can be read out before program confirm command(10h). The sequence is as follow.
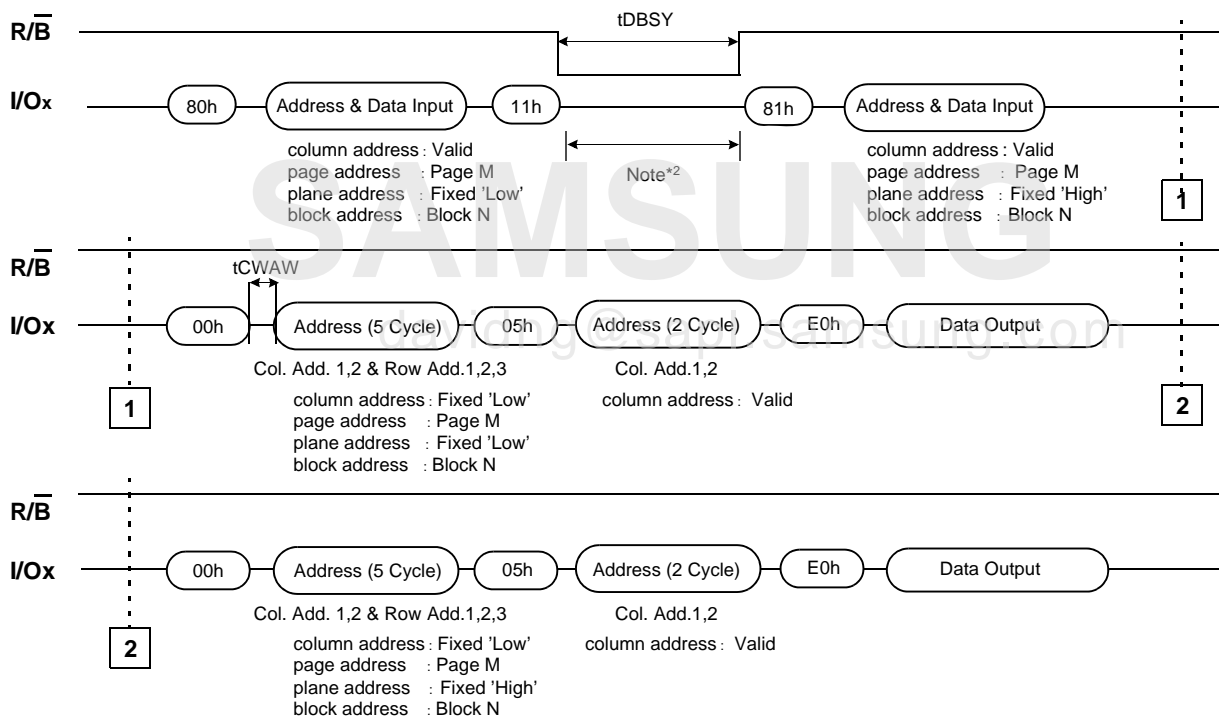
Register Read Out

R/B

tCWAW

I/Ox 80h Address & Data Input 00h Address 05h Address E0h Data Output

Col Add1,2 & Row Add1,2,3 Date

Col Add1,2 & Row Add1,2,3

Col Add1,2

NOTE :
Register read out operation is prohibited during cache program operation.

5.10 Two-plane Register Read Out Mode 1

At two-plane program operation, loaded data to the register can be read out before program confirm command(10h). The sequence is as follow.

Two-Plane Register Read Out Mode 1

R/B tDBSY

I/Ox 80h Address & Data Input 11h 81h Address & Data Input

column address : Valid
page address : Page M
plane address : Fixed 'Low'
block address : Block N

Note*2

column address : Valid
page address : Page M
plane address : Fixed 'High'
block address : Block N

1

R/B tCWAW

I/Ox 00h Address (5 Cycle) 05h Address (2 Cycle) E0h Data Output

Col. Add. 1,2 & Row Add.1,2,3

Col. Add.1,2

1

column address : Fixed 'Low'
page address : Page M
plane address : Fixed 'Low'
block address : Block N

column address : Valid

2

R/B

I/Ox 00h Address (5 Cycle) 05h Address (2 Cycle) E0h Data Output

Col. Add. 1,2 & Row Add.1,2,3

Col. Add.1,2

2

column address : Fixed 'Low'
page address : Page M
plane address : Fixed 'High'
block address : Block N
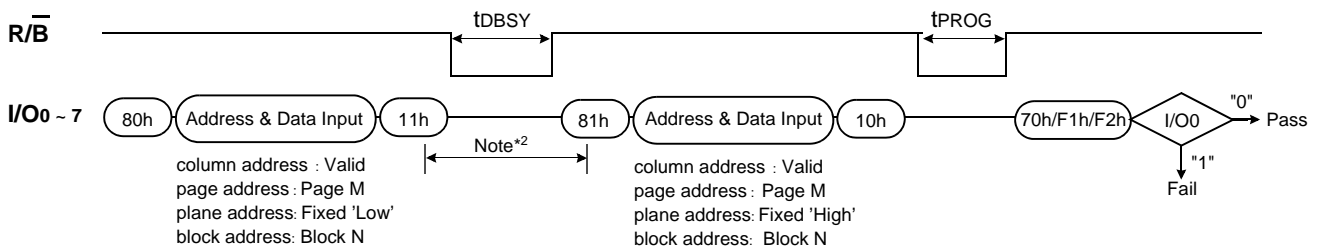
column address : Valid

NOTE :
1) It is noticeable that physically same row address is applied to two planes .
2) Any command between 11h and 81h is prohibited except 70h/F1h/F2h and FFh.
3) Register read out operation is prohibited during cache program operation.

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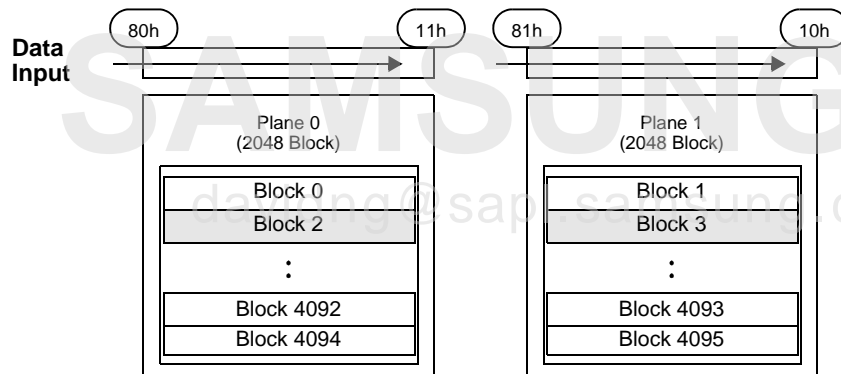
FLASH MEMORY

5.11 Two-plane Page Program

Two-Plane Page Program is an extension of Page Program, for a single plane with 8,704 byte data registers. Since the device is equipped with two memory planes, activating the two sets of 8,704 byte data registers enables a simultaneous programming of two pages.

After writing the first set of data up to 8,704 byte into the selected data registers via cache registers, Dummy Page Program command (11h) instead of actual Page Program command (10h) is inputted to finish data-loading of the first plane. Since no programming process is involved, R/B remains in Busy state for a short period of time(tDBSY). Read Status command (70h/F1h/F2h) may be issued to find out when the device returns to Ready state by polling the Ready/Busy status bit(I/O 6). Then the next set of data for the other plane is inputted after the 81h command and address sequences. After inputting data for the last plane, actual True Page Program(10h) instead of dummy Page Program command (11h) must be followed to start the programming process. The operation of R/B and Read Status is the same as that of Page Program. Although two planes are programmed simultaneously, pass/fail is not available for each page when the program operation completes. Status bit of I/O 0 is set to "1" when any of the pages fails.

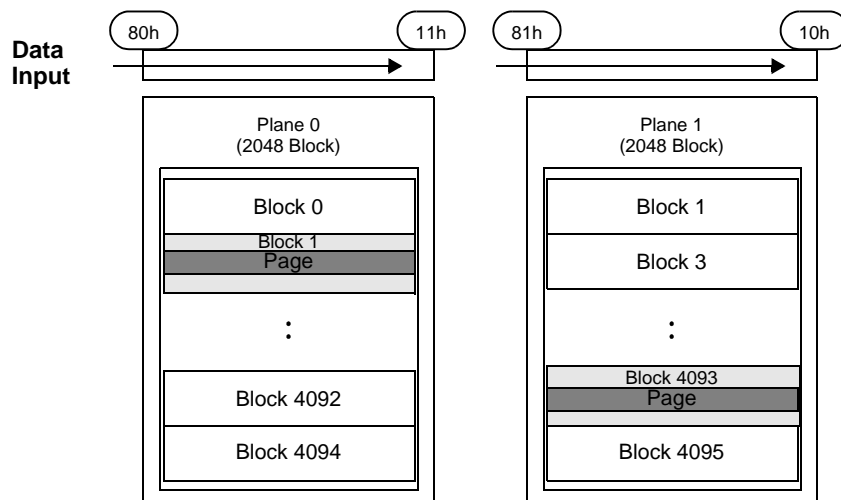Restriction in addressing with Two-Plane Page Program is shown below.

Two-Plane Page Program

R/B

tDBSY   tPROG

I/O0 ~ 7

80h — Address & Data Input — 11h — Note*2 — 81h — Address & Data Input — 10h — 70h/F1h/F2h — I/O0 — "0" Pass / "1" Fail

column address : Valid
page address : Page M
plane address: Fixed 'Low'
block address: Block N

column address : Valid
page address : Page M
plane address: Fixed 'High'
block address: Block N

NOTE :
1) It is noticeable that same row address except for the Plane address is applied to the two blocks
2) Any command between 11h and 81h is prohibited except 70h/F1h/F2h and FFh.

Data Input

80h ... 11h   81h ... 10h

Plane 0 (2048 Block)

Block 0
Block 2
:
Block 4092
Block 4094

Plane 1 (2048 Block)

Block 1
Block 3
:
Block 4093
Block 4095

Unaligned Two- Plane Page Program

Data Input

80h ... 11h   81h ... 10h

Plane 0 (2048 Block)

Block 0
Block 1
Page
:
Block 4092
Block 4094

Plane 1 (2048 Block)

Block 1
Block 3
:
Block 4093
Page
Block 4095

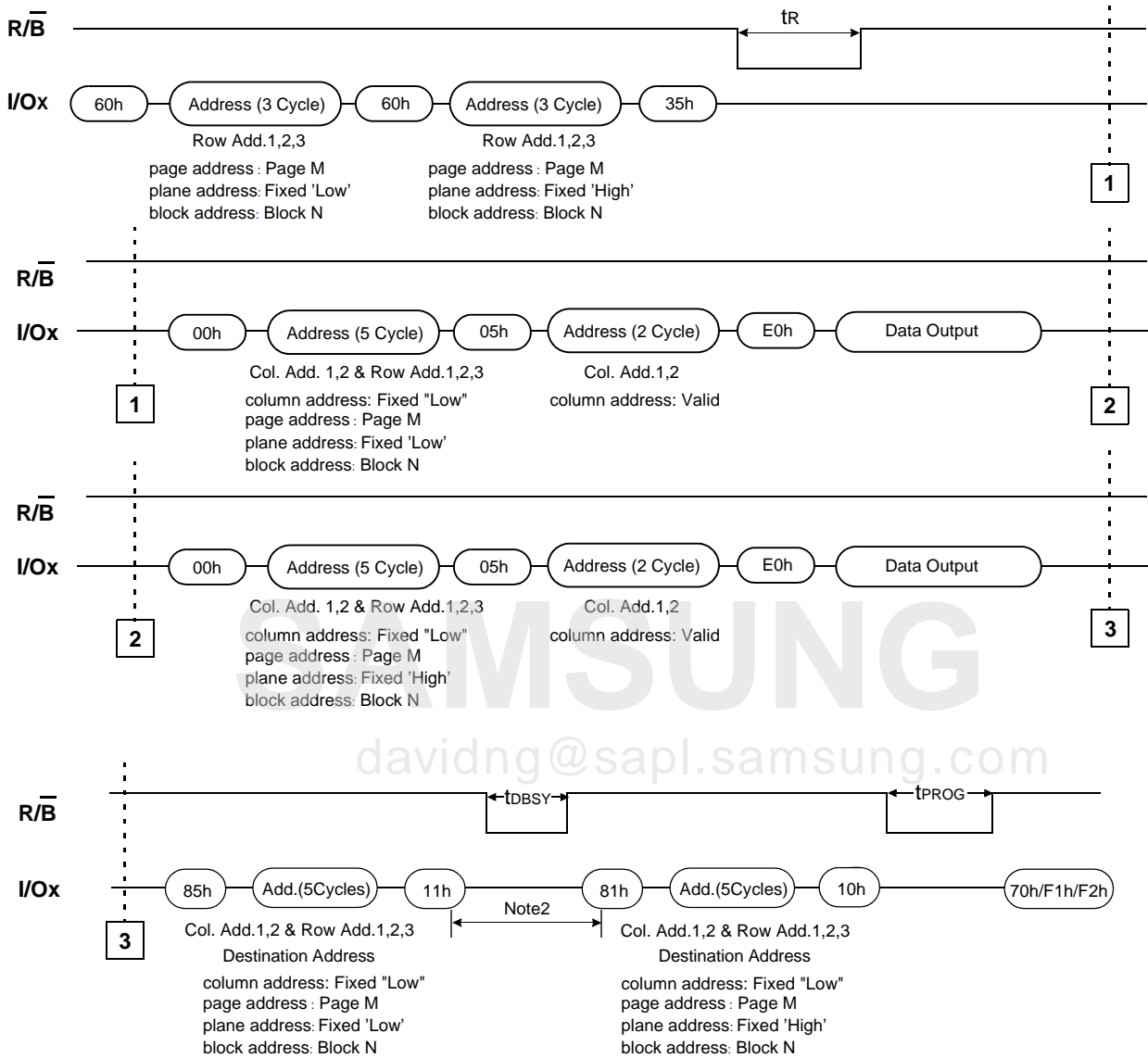**NOTE :**
1) Two-Plane page Program operation shall be supported in unaligned block address, as long as address are same in all pages.

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5.12 Two-plane Copy-back Program

Two-Plane Copy-Back Program is an extension of Copy-Back Program, for a single plane with 8,704 byte data registers. Since the device is equipped with two memory planes, activating the two sets of 8,704 byte data registers enables a simultaneous programming of two pages.

Two-Plane Copy-Back Program Operation

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```
            Plane0                      Plane1

        Source page                  Source page

        Target page                  Target page         (1) : Two-Plane Read for Copy Back
                                                          (2) : Two-Plane Random Data Out
         (1)      (3)                  (1)      (3)        (3) : Two-Plane Copy-Back Program


        Data Field   Spare Field      Data Field   Spare Field
     (2)                           (2)
```

NOTE :
1) Copy-Back Program operation is allowed only within the same memory plane.
2) Any command between 11h and 81h is prohibited except 70h/F1h/F2h and FFh.
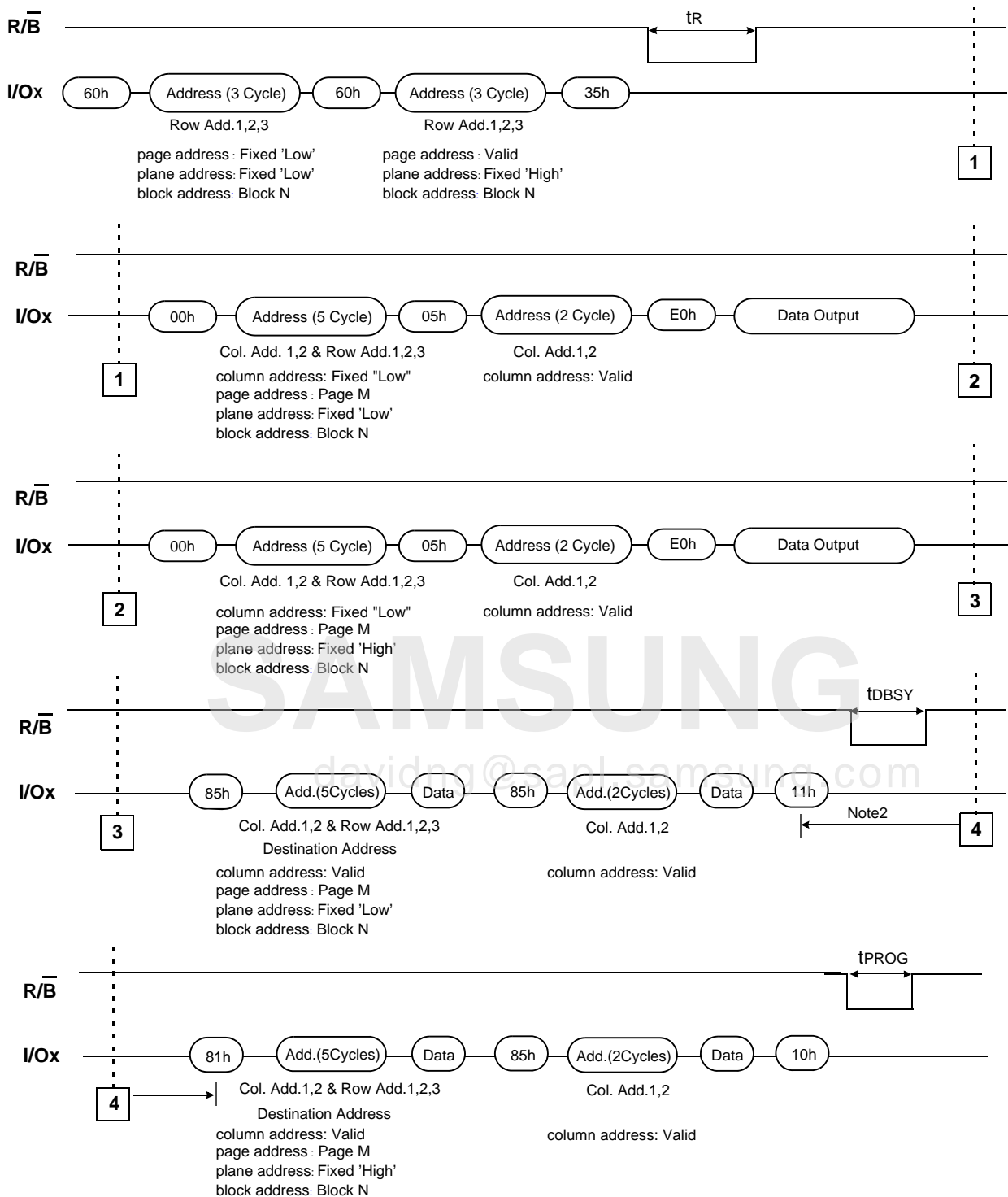
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Two-Plane Copy-Back Program Operation with Random Data Input

$R/\overline{B}$

tR

I/Ox: 60h — Address (3 Cycle) — 60h — Address (3 Cycle) — 35h

Row Add.1,2,3 — Row Add.1,2,3

page address : Fixed 'Low'
plane address: Fixed 'Low'
block address: Block N

page address : Valid
plane address: Fixed 'High'
block address: Block N

1

$R/\overline{B}$

I/Ox: 00h — Address (5 Cycle) — 05h — Address (2 Cycle) — E0h — Data Output

Col. Add. 1,2 & Row Add.1,2,3 — Col. Add.1,2

column address: Fixed "Low"
page address : Page M
plane address: Fixed 'Low'
block address: Block N

column address: Valid

1 ... **2**

$R/\overline{B}$

I/Ox: 00h — Address (5 Cycle) — 05h — Address (2 Cycle) — E0h — Data Output

Col. Add. 1,2 & Row Add.1,2,3 — Col. Add.1,2

column address: Fixed "Low"
page address : Page M
plane address: Fixed 'High'
block address: Block N

column address: Valid

2 ... **3**

$tDBSY$

$R/\overline{B}$

I/Ox: 85h — Add.(5Cycles) — Data — 85h — Add.(2Cycles) — Data — 11h

Col. Add.1,2 & Row Add.1,2,3 — Col. Add.1,2
Destination Address

column address: Valid
page address : Page M
plane address: Fixed 'Low'
block address: Block N

column address: Valid

Note2

3 ... **4**

$tPROG$

$R/\overline{B}$

I/Ox: 81h — Add.(5Cycles) — Data — 85h — Add.(2Cycles) — Data — 10h

Col. Add.1,2 & Row Add.1,2,3 — Col. Add.1,2
Destination Address

column address: Valid
page address : Page M
plane address: Fixed 'High'
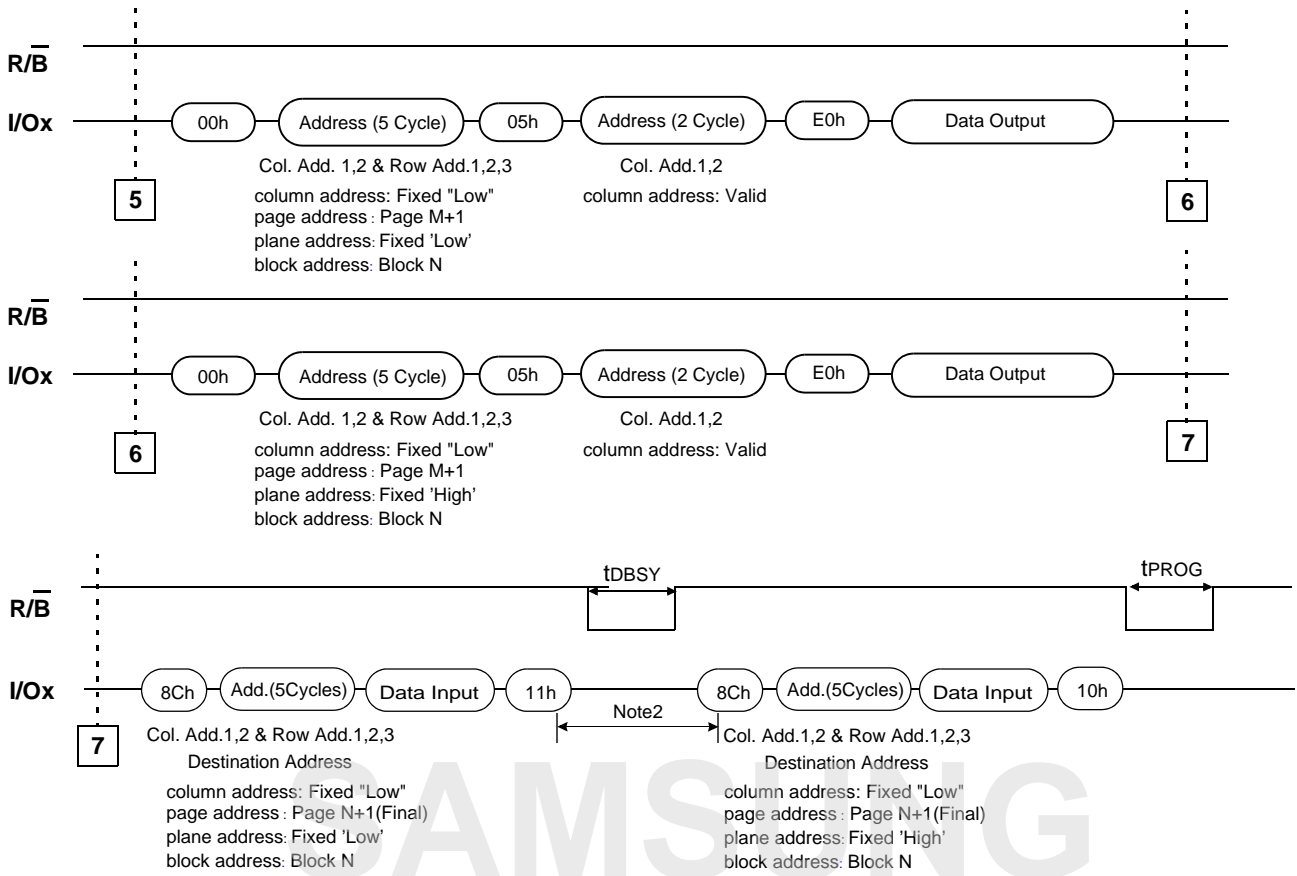block address: Block N

column address: Valid

4

NOTE :
1) Copy-Back Program operation is allowed only within the same memory plane.
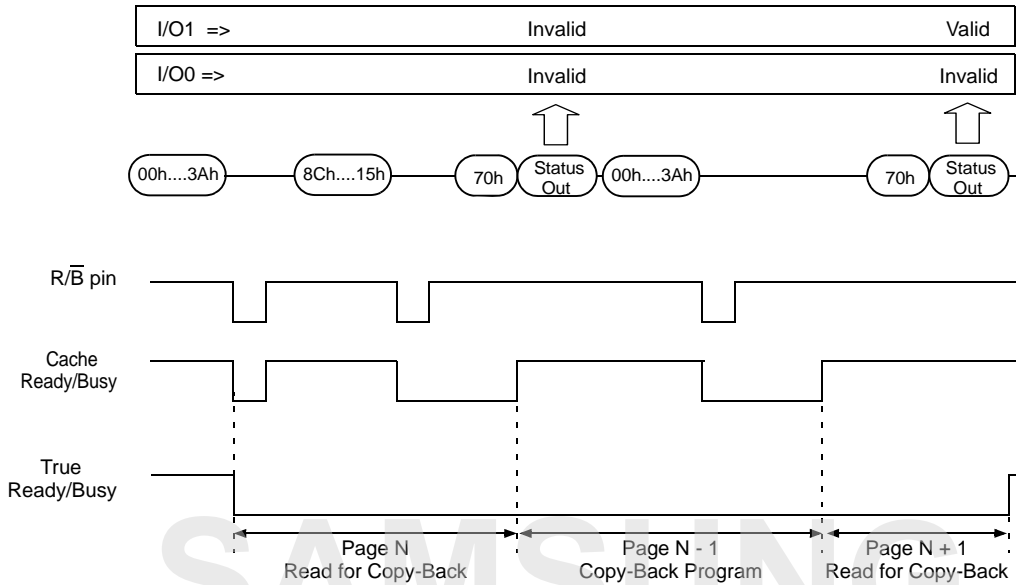2) Any command between 11h and 81h is prohibited except 70h/F1h/F2h and FFh.

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5.13 Two-Plane Intelligent Copy-back Program(1/2)

Two-Plane Intelligent Copy-Back Program Operation

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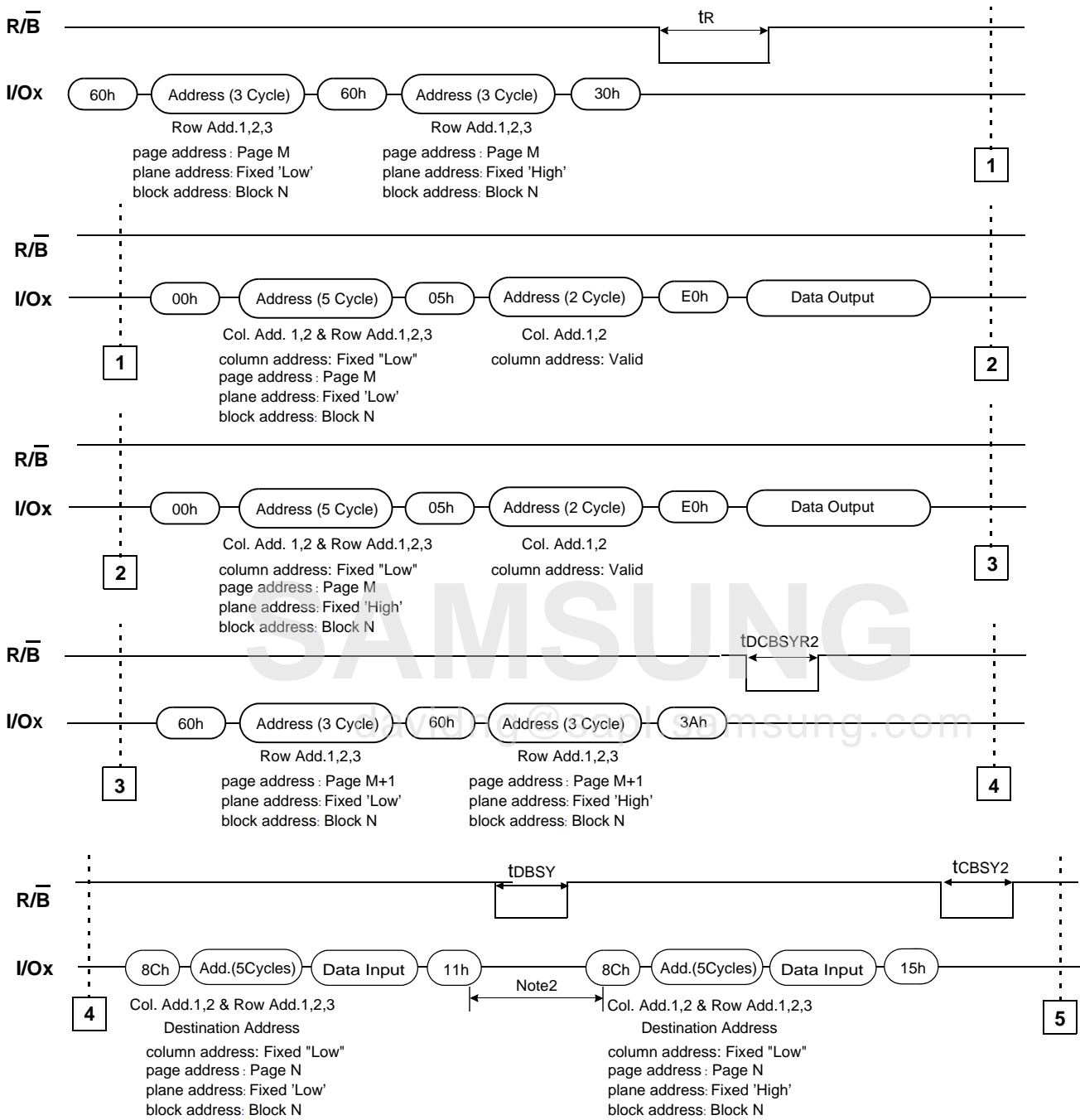
Two-Plane Intelligent Copy-back Program(2/2)

NOTE :
1) Two-Plane Intelligent Copy-Back Program operation is allowed only within the same memory plane.
2) Any command between 11h and 8Ch is prohibited except 70h/F1h/F2h and FFh.

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Pass/Fail status for each page programmed by the Intelligent Copy-Back Program operation can be detected by the Read Status operation.
- I/O 0 : Pass/Fail of the current page program operation.
- I/O 1 : Pass/Fail of the previous page program operation.

The Pass/Fail status on I/O 0 and I/O 1 are valid under the following conditions.
- Status on I/O 0 : True Ready/Busy is Ready state.
    The True Ready/Busy is output on I/O 5 by Read Status operation or R/$\overline{B}$ pin after the 10h command.
- Status on I/O 1 :Cache Ready/Busy is Ready State.
    The Cache Ready/Busy is output on I/O 6 by Read Status operation or R/$\overline{B}$ pin after the 15h command.

CASE 1

CASE 2

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FLASH MEMORY
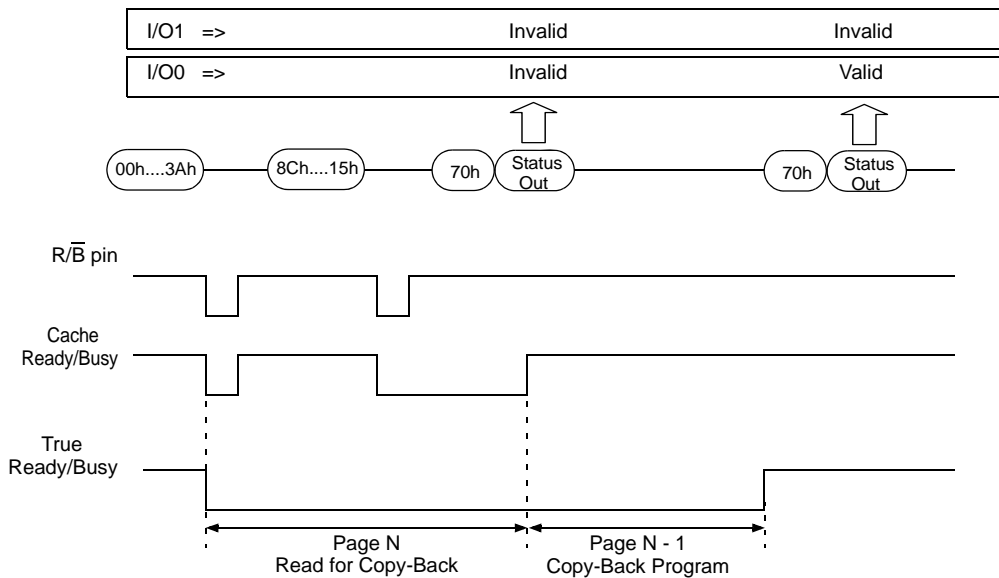
5.14 Two-plane Cache Program

Two-Plane Cache Program is an extension of Cache Program, for a single plane with 8,704 byte data registers. Since the device is equipped with two memory planes, activating the two sets of 8,704 byte data registers enables a simultaneous programming of two pages.

Two-Plane Cache Program Operation
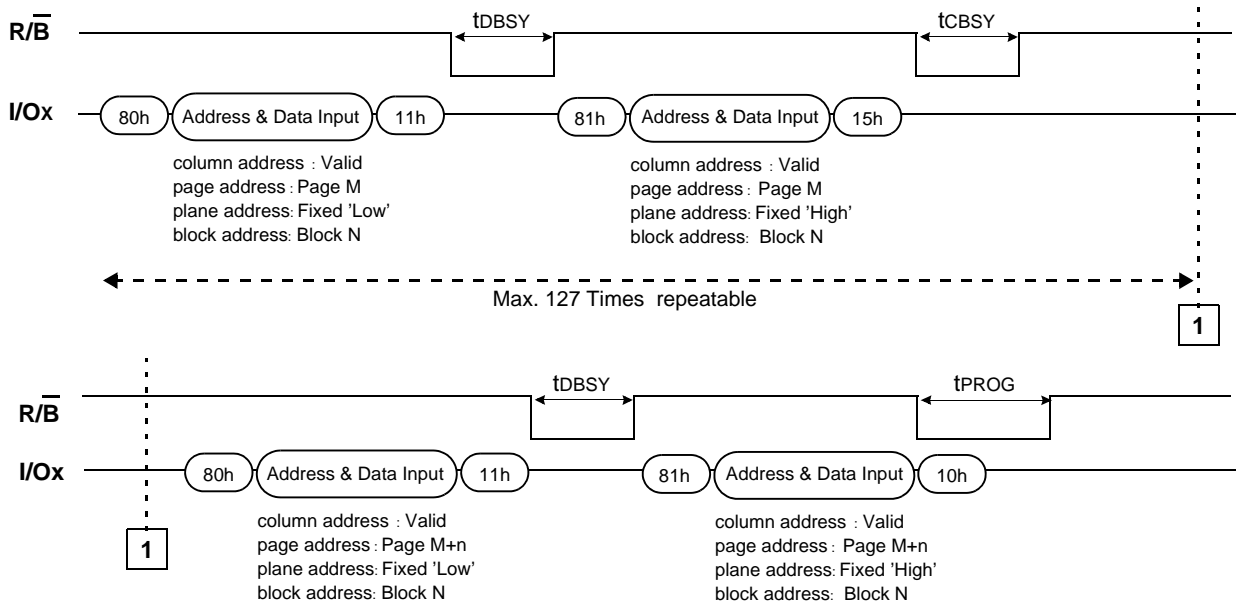
NOTE :
1) It is noticeable that same row address except for the Plane address is applied to the two blocks
2) Any command between 11h and 81h is prohibited except 70h/F1h/F2h and FFh.
3) Since programming the last page does not employ caching, the program time has to be that of Page Program. However, if the previous program cycle with the cache data has not finished, the actual program cycle of the last page is initiated only after completion of the previous cycle, which can be expressed as the following formula.

tPROG = Program time for the last page + Program time for the (last -1)th page
- (Program command cycle time + Last page data loading time)

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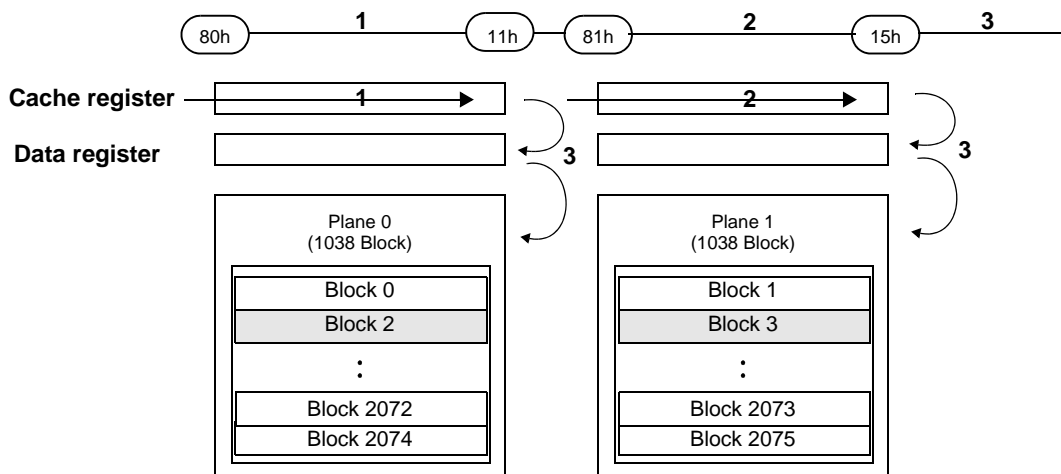
5.15 Block Erase

The Erase operation is done on a block basis. Block address loading is accomplished in three cycles initiated by an Erase Setup command(60h). Only Plane address and Block address are valid while Page address is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit(I/O 0) may be checked.
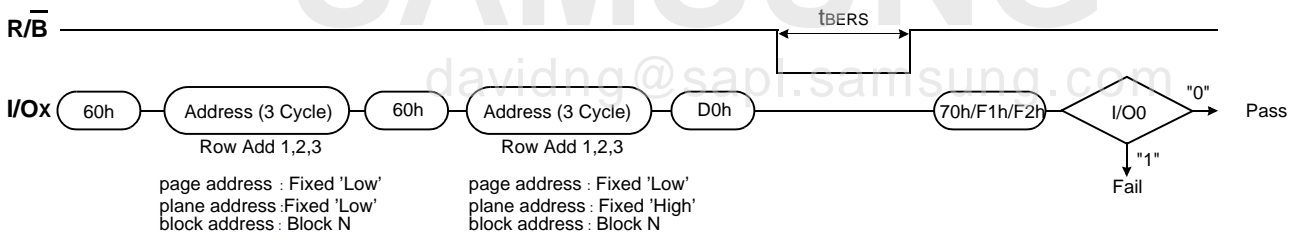
Block Erase Operation
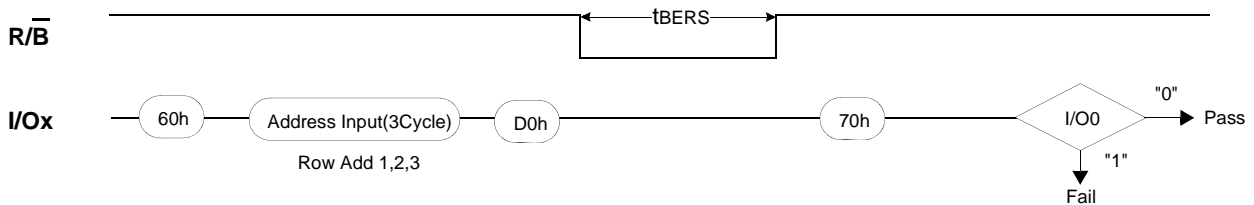
5.16 Two-plane Block Erase

Basic concept of Two-Plane Block Erase operation is identical to that of Two-Plane Page Program. Up to two blocks, one from each plane can be simultaneously erased. Standard Block Erase command sequences (Block Erase Setup command(60h) followed by three address cycles) may be repeated up to twice for erasing up to two blocks. Only one block should be selected from each plane. The Erase Confirm command(D0h) initiates the actual erasing process. The completion is detected by monitoring R/$\overline{B}$ pin or Ready/Busy status bit (I/O 6).

Two-Plane Block Erase Operation

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5.17 Read Status

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h or F1h/F2h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE or RE, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/B pins are common-wired. RE or CE does not need to be toggled for updated status. Refer to the table for specific 70h Status Register definitions and F1h/F2h status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command(00h) should be given before starting read cycles.

Status Register Definition for 70h Command

I/O	Page Program	Block Erase	Cache Program	Intelligent Copy-Back Program	Read	Cache Read	Intelligent Copy-Back Read	Definition
I/O 0	Pass/Fail	Pass/Fail	Pass/Fail(N)	Pass/Fail(N)	Not Use	Not Use	Not Use	Pass : "0" Fail : "1"
I/O 1	Not Use Use	Not Use Use	Pass/Fail(N-1) District 0 Pass/Fail	Pass/Fail(N-1) District 0 Pass/Fail	Not Use District 0 Pass/Fail	Not Use	Not Use	Pass : "0" Fail : "1"
I/O 2	Not Use District 0 Pass/Fail	Not Use District 0 Pass/Fail	Not Use District 0 Pass/Fail	Not Use District 0 Pass/Fail	Not Use District 0 Pass/Fail	Not Use	Not Use	Don't -cared
I/O 3	Not Use	Not Use	Not Use	Not Use	Not Use	Not Use	Not Use	Don't -cared
I/O 4	Not Use	Not Use	Not Use	Not Use	Not Use	Not Use	Not Use	Don't -cared
I/O 5	Not Use	Not Use	True Ready/Busy	True Ready/Busy	Not Use	True Ready/Busy	True Ready/Busy	Busy : "0" Ready : "1"
I/O 6	Ready/Busy	Ready/Busy	Cache Ready/Busy	Cache Ready/Busy	Ready/Busy	Cache Ready/Busy	Cache Ready/Busy	Busy : "0" Ready : "1"
I/O 7	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Protected : "0" Not Protected : "1"

NOTE :
1) I/Os defined 'Not use' are recommended to be masked out when Read Status is executed.
2) N : current page,   N-1: previous page.

Status Register Definition for F1h Command

I/O	Page Program	Block Erase	Cache Program	Intelligent Copy-Back Program	Read	Cache Read	Intelligent Copy-Back Read	Definition
I/O 0	Chip1 Pass/Fail	Chip1 Pass/Fail	Chip1 Pass/Fail(N)	Chip1 Pass/Fail(N)	Not Use	Not Use	Not Use	Pass : "0" Fail : "1"
I/O 1	Plane0 Pass/Fail	Plane0 Pass/Fail	Plane0 Pass/Fail(N)	Plane0 Pass/Fail(N)	Not Use	Not Use	Not Use	Pass : "0" Fail : "1"
I/O 2	Plane1 Pass/Fail	Plane1 Pass/Fail	Plane1 Pass/Fail(N)	Plane1 Pass/Fail(N)	Not Use	Not Use	Not Use	Pass : "0" Fail : "1"
I/O 3	Not Use	Not Use	Plane0 Pass/Fail(N-1)	Plane0 Pass/Fail(N-1)	Not Use	Not Use	Not Use	Pass : "0" Fail : "1"
I/O 4	Not Use	Not Use	Plane1 Pass/Fail(N-1)	Plane1 Pass/Fail(N-1)	Not Use	Not Use	Not Use	Pass : "0" Fail : "1"
I/O 5	Not Use	Not Use	True Ready/Busy	True Ready/Busy	Not Use	True Ready/Busy	True Ready/Busy	Busy : "0" Ready : "1"
I/O 6	Ready/Busy	Ready/Busy	Cache Ready/Busy	Cache Ready/Busy	Ready/Busy	Cache Ready/Busy	Cache Ready/Busy	Busy : "0" Ready : "1"
I/O 7	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Protected : "0" Not Protected : "1"

NOTE :
1) I/Os defined 'Not use' are recommended to be masked out when Read Status is being executed.
2) N : current page,   N-1 : previous page.

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Status Register Definition for F2h Command

I/O	Page Program	Block Erase	Cache Program	Intelligent Copy-Back Program	Read	Cache Read	Intelligent Copy-Back Read	Definition
I/O 0	Chip2 Pass/Fail	Chip2 Pass/Fail	Chip2 Pass/Fail(N)	Chip2 Pass/Fail(N)	Not Use	Not Use	Not Use	Pass : "0" Fail : "1"
I/O 1	Plane0 Pass/Fail	Plane0 Pass/Fail	Plane0 Pass/Fail(N)	Plane0 Pass/Fail(N)	Not Use	Not Use	Not Use	Pass : "0" Fail : "1"
I/O 2	Plane1 Pass/Fail	Plane1 Pass/Fail	Plane1 Pass/Fail(N)	Plane1 Pass/Fail(N)	Not Use	Not Use	Not Use	Pass : "0" Fail : "1"
I/O 3	Not Use	Not Use	Plane0 Pass/Fail(N-1)	Plane0 Pass/Fail(N-1)	Not Use	Not Use	Not Use	Pass : "0" Fail : "1"
I/O 4	Not Use	Not Use	Plane1 Pass/Fail(N-1)	Plane1 Pass/Fail(N-1)	Not Use	Not Use	Not Use	Pass : "0" Fail : "1"
I/O 5	Not Use	Not Use	True Ready/Busy	True Ready/Busy	Not Use	True Ready/Busy	True Ready/Busy	Busy : "0" Ready : "1"
I/O 6	Ready/Busy	Ready/Busy	Cache Ready/Busy	Cache Ready/Busy	Ready/Busy	Cache Ready/Busy	Cache Ready/Busy	Busy : "0" Ready : "1"
I/O 7	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Protected : "0" Not Protected : "1"

NOTE :
1) I/Os defined 'Not use' are recommended to be masked out when Read Status is being executed.
2) N : current page,   N-1 : previous page.

5.18 Read Id

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Six read cycles sequentially output the manufacturer code(ECh), and the device code and 3rd, 4th, 5th, 6th cycle ID respectively. The command register remains in Read ID mode until further commands are issued to it.

Read ID Operation
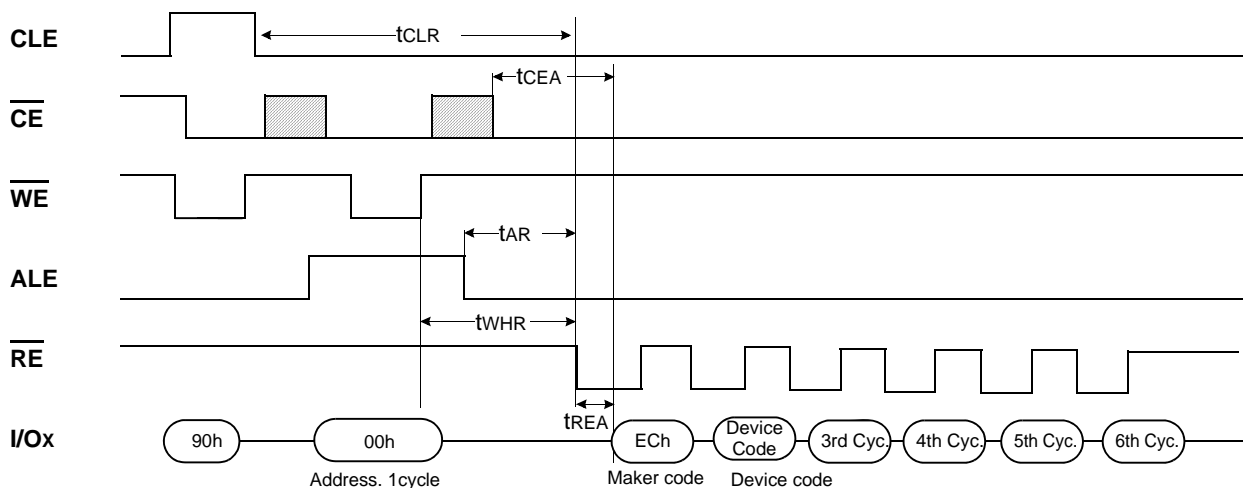
Device	1st Cycle	Dvice Code(2nd)	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
K9GBG08U0B	ECh	D7h	94h	7Eh	64h	44h
K9LCG08U0B	ECh	DEh	D5h	7Eh	68h	44h

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5.19 Reset

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when WP is high. Refer to table for device status after reset operation. If the device is already in reset state a new reset command will be accepted by the command register. The R/B pin changes to low for tRST after the Reset command is written.

RESET Operation
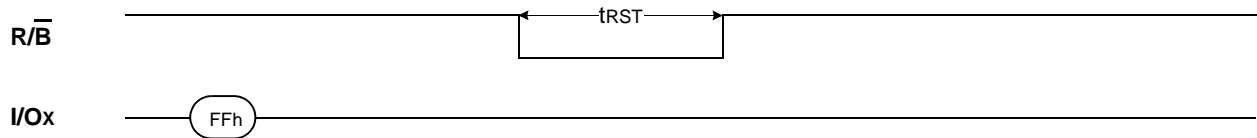
Device Status

	After Power-up	After Reset
Operation mode Mode	00h Command is latched	Waiting for next command

5.20 Output driver setting

The device supports four kinds of output driver setting for matching the system characteristics. The nominal output drive strength is the power-on default value. The host is able to select a different drive strength setting using the SET FEATURES (EFh) command with following 10h address (driver setting feature address). The output impedance range from minimum to maximum covers process, voltage, and temperature variations. Devices are not guaranteed to be at the nominal value. The users can tune the output driver impedance of the data by setting the driver strength register value. (See Configuration Register Table) Table 5 shows which output driver would be tuned and the strength according to setting data. Upon power-up, the register will revert to the default setting. Table 6 & Table 7 shows the output driver strength impedance values of each strength and pull-up and pull down output impedance mismatch.

Driver Strength Register Setting
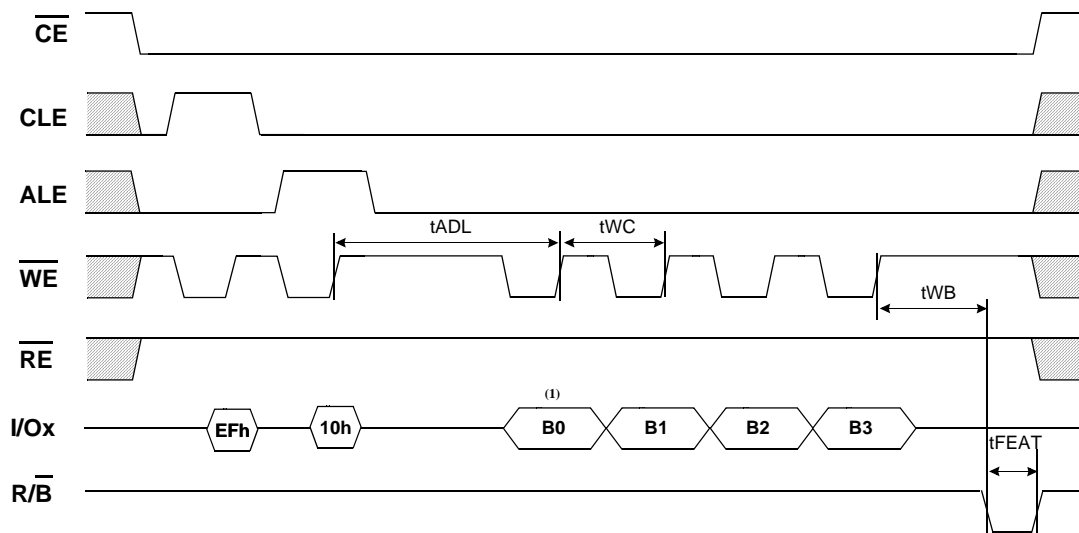
NOTE :
1) B0-B3 are parameters identifying new settings for the feature specified.

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[Table 4] Output Driver Setting

B0 Value	Driver Strength
00h~01h	Reserved
02h	Driver Multiplier : underdriver1
03h	Reserved
04h	Driver Multiplier : 1 (default)
05h	Reserved
06h	Driver Multiplier :overdriver1
07h	Reserved
09h	Reserved
0Ah ~FFh	Reserved

[Table 5] Output Drive Strength Impedance Values

Output Strength	Rpd/Rpu	VOUT to VssQ	Minimum	Nominal	Maximum	Units
			VccQ(3.3V)	VccQ(3.3V)	VccQ(3.3V)	
Overdrive1	Rpd	VccQ × 0.2	18	27	43	ohms
		VccQ × 0.5	20	32	53	ohms
		VccQ × 0.8	29	46	77	ohms
	Rpu	VccQ × 0.2	29	46	77	ohms
		VccQ × 0.5	20	32	53	ohms
		VccQ × 0.8	18	27	43	ohms
Nominal	Rpd	VccQ × 0.2	23	34	54	ohms
		VccQ × 0.5	26	40	68	ohms
		VccQ × 0.8	36	57	96	ohms
	Rpu	VccQ × 0.2	36	57	96	ohms
		VccQ × 0.5	26	40	68	ohms
		VccQ × 0.8	23	34	54	ohms
Underdrive	Rpd	VccQ × 0.2	30	45	72	ohms
		VccQ × 0.5	34	53	91	ohms
		VccQ × 0.8	48	76	128	ohms
	Rpu	VccQ × 0.2	48	76	128	ohms
		VccQ × 0.5	34	53	91	ohms
		VccQ × 0.8	30	45	72	ohms

[Table 6] Pull-up and Pull-down Output Impedance Mismatch

| Drive Strength	Min	Max	Unit	Notes
	VccQ(3.3V)	VccQ(3.3V)		
Overdrive 1	0	8	ohms	1, 2
Nominal	0	10	ohms	1, 2
Underdrive	0	14	ohms	1, 2

NOTE :
1) Mismatch is the absolute value between pull-up and pull-down impedances. Both are measured at the same temperature and voltage.
2) Test conditions: VccQ = VccQ(min), Vout = VccQ × 0.5, $T_A = T_{OPER}$

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5.21 Ready/$\overline{busy}$

The device has a R/$\overline{B}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{B}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. Because pull-up resistor value is related to tr(R/$\overline{B}$) and current drain during busy(ibusy) , an appropriate value can be obtained with the following reference chart. Its value can be determined by the following guidance.
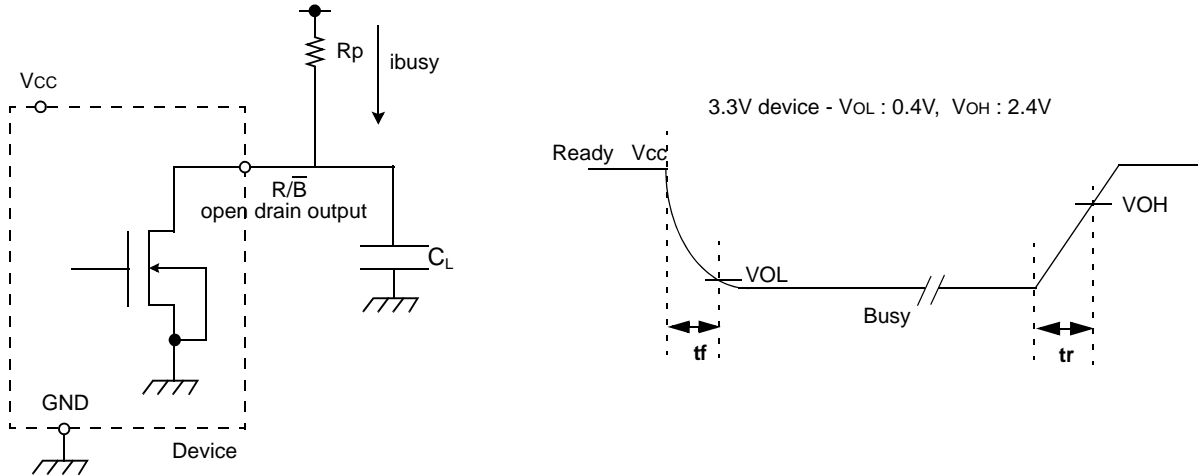
### Rp vs tr ,tf & Rp vs ibusy
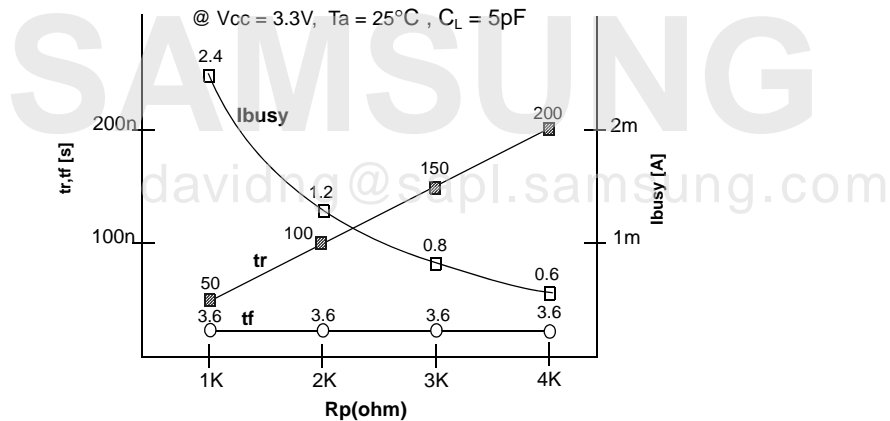
Rp value guidance

$$Rp(min, 3.3V\ part) = \frac{VCC(Max.) - VOL(Max.)}{IOL + \Sigma IL} = \frac{3.2V}{8mA + \Sigma IL}$$

where I_L is the sum of the input currents of all devices tied to the R/$\overline{B}$ pin.
Rp(max) is determined by maximum permissible limit of tr

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6.0 DATA PROTECTION & POWER UP SEQUENCE

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 2V. The Reset command(FFh) must be issued to all $\overline{CE}$s as the first command after the NAND Flash device is powered on. Each $\overline{CE}$ will be busy for a maximum of 5ms after a RESET command is issued. In this time period, the acceptable command is 70h/F1h/F2h.
$\overline{WP}$ pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down. The two step command sequence for program/erase provides additional software protection.

AC Waveforms for Power Transition
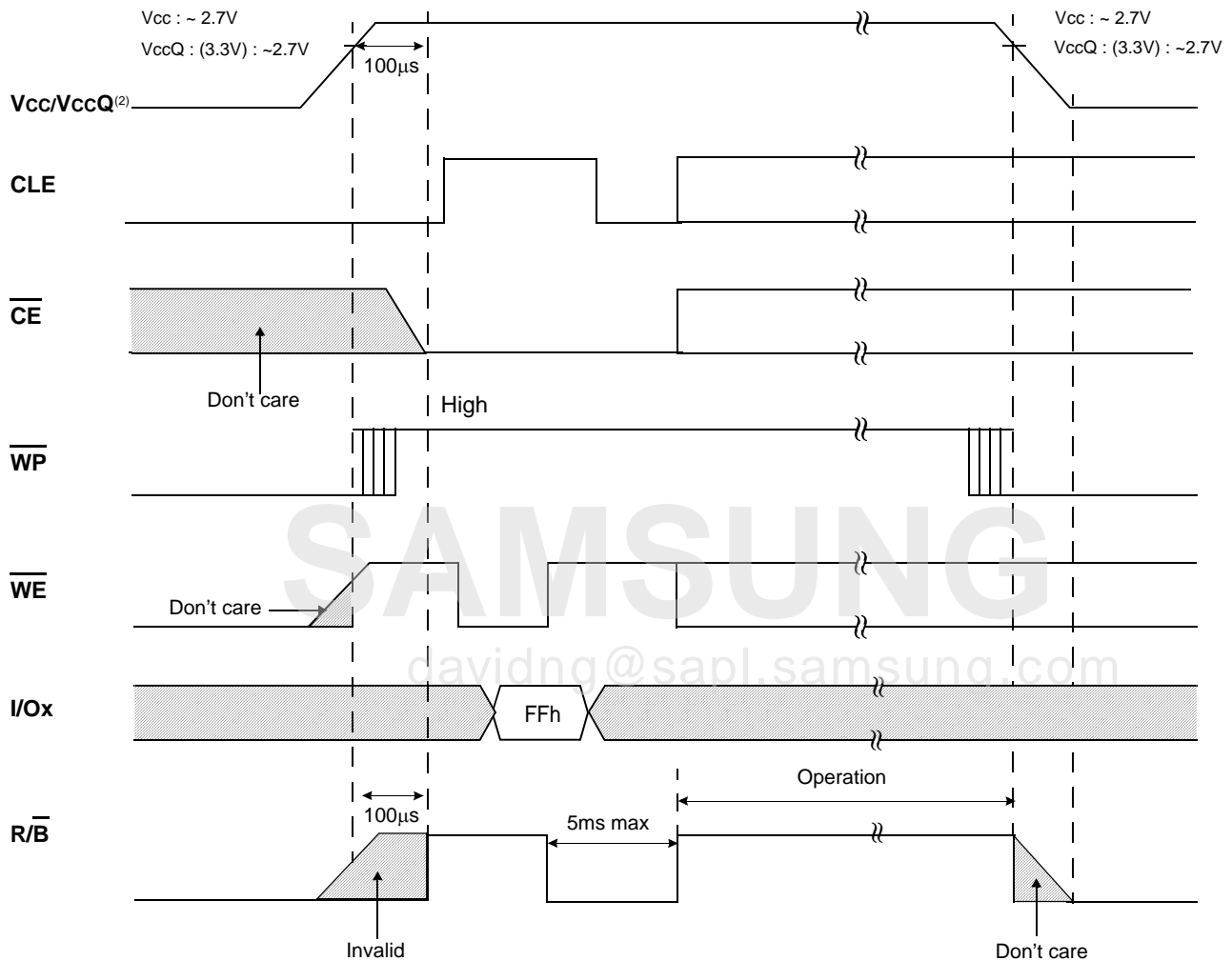
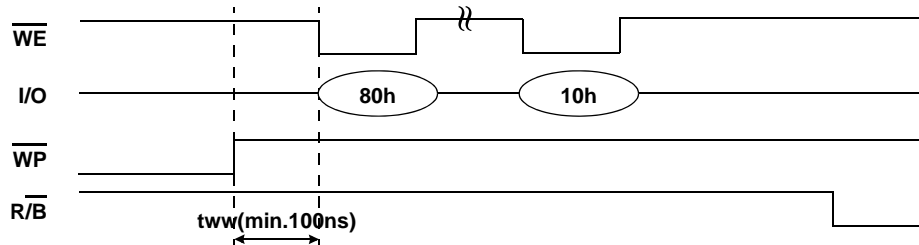**NOTE :**
1) During the initialization, the device consumes a maximum current of 50mA (ICC1)
2) Vcc should be reached the valid voltage no later than VccQ.

SAMSUNG CONFIDENTIAL

Rev. 1.0

K9GBG08U0B
K9LCG08U0B

datasheet

FLASH MEMORY

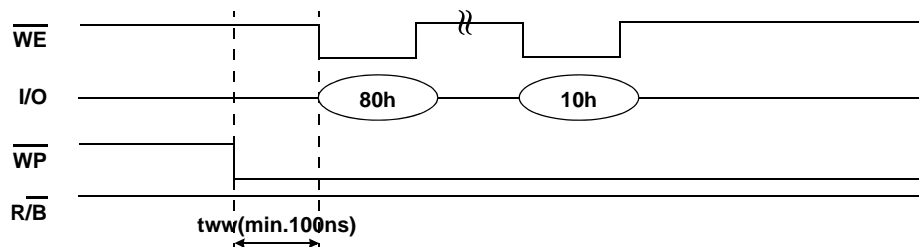# 6.1 $\overline{WP}$ AC Timing guide

Enabling $\overline{WP}$ during erase and program busy is prohibited. The erase and program operations are enabled and disabled as follows:
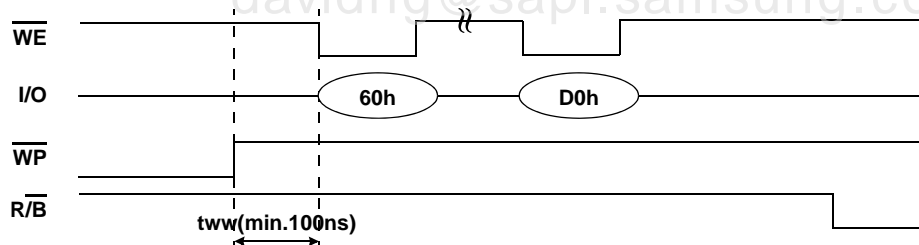
Program Operation

1. Enable Mode

$\overline{WE}$	
I/O	80h 10h
$\overline{WP}$	
R/$\overline{B}$	tww(min.100ns)

2. Disable Mode

$\overline{WE}$	
I/O	80h 10h
$\overline{WP}$	
R/$\overline{B}$	tww(min.100ns)

Erase Operation

1. Enable Mode

$\overline{WE}$	
I/O	60h D0h
$\overline{WP}$	
R/$\overline{B}$	tww(min.100ns)

2. Disable Mode

$\overline{WE}$	
I/O	60h D0h
$\overline{WP}$	
R/$\overline{B}$	tww(min.100ns)